

Journée Common - Geneve Dec 2013



IBM Power Systems Trends & Direction

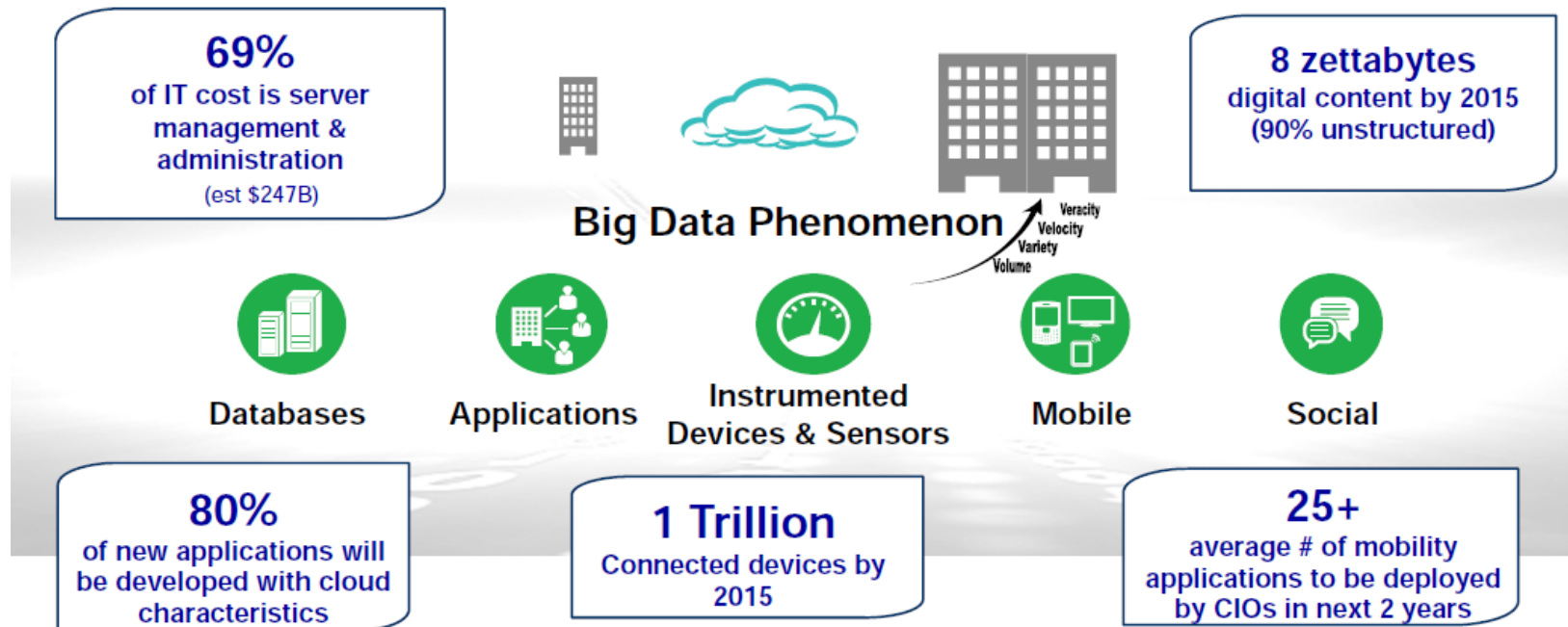
*Beyond
Power7*

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Business-needs and Workloads are Transforming

Driving infrastructure transformation



1 ZB =
100000000000000000000000bytes =
1000⁷bytes = 10²¹bytes =
1000exabytes = 1 billion terabytes

Client Business needs have evolved

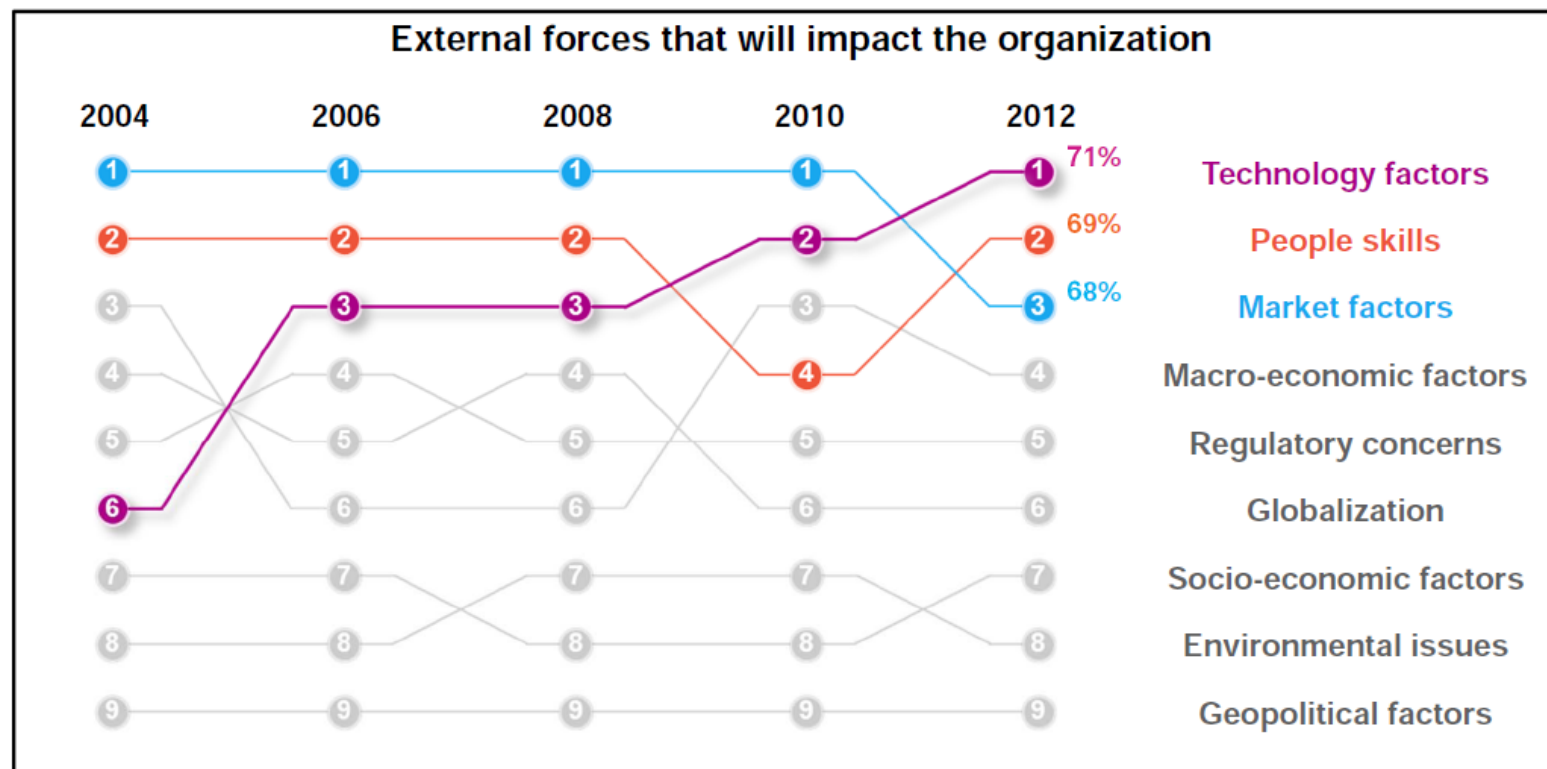
- Data-driven insights
- Flexible, responsive IT environment
- Secure from external and internal threats
- Simplified end user experience
- Compelling ROI

Multiples of bytes			
Decimal		Binary	
Value	Metric	Value	JEDEC
1000 KB	kilobyte	1024 KB	Kilobyte
1000 ² MB	megabyte	1024 ² MB	Megabyte
1000 ³ GB	gigabyte	1024 ³ GB	Gigabyte
1000 ⁴ TB	terabyte	1024 ⁴ TB	Terabyte
1000 ⁵ PB	petabyte	1024 ⁵	PB
1000 ⁶ EB	exabyte	1024 ⁶	EiB
1000 ⁷ ZB	zettabyte	1024 ⁷	ZiB
1000 ⁸ YB	yottabyte	1024 ⁸	YiB



Technology: critical to the success of the business

- For the first time, CEOs identify technology as the most important external force impacting their organizations



Source: Q1 IBM CEO study 2012 "What are the most important external forces that will impact your organization over the next 3 to 5 years?"

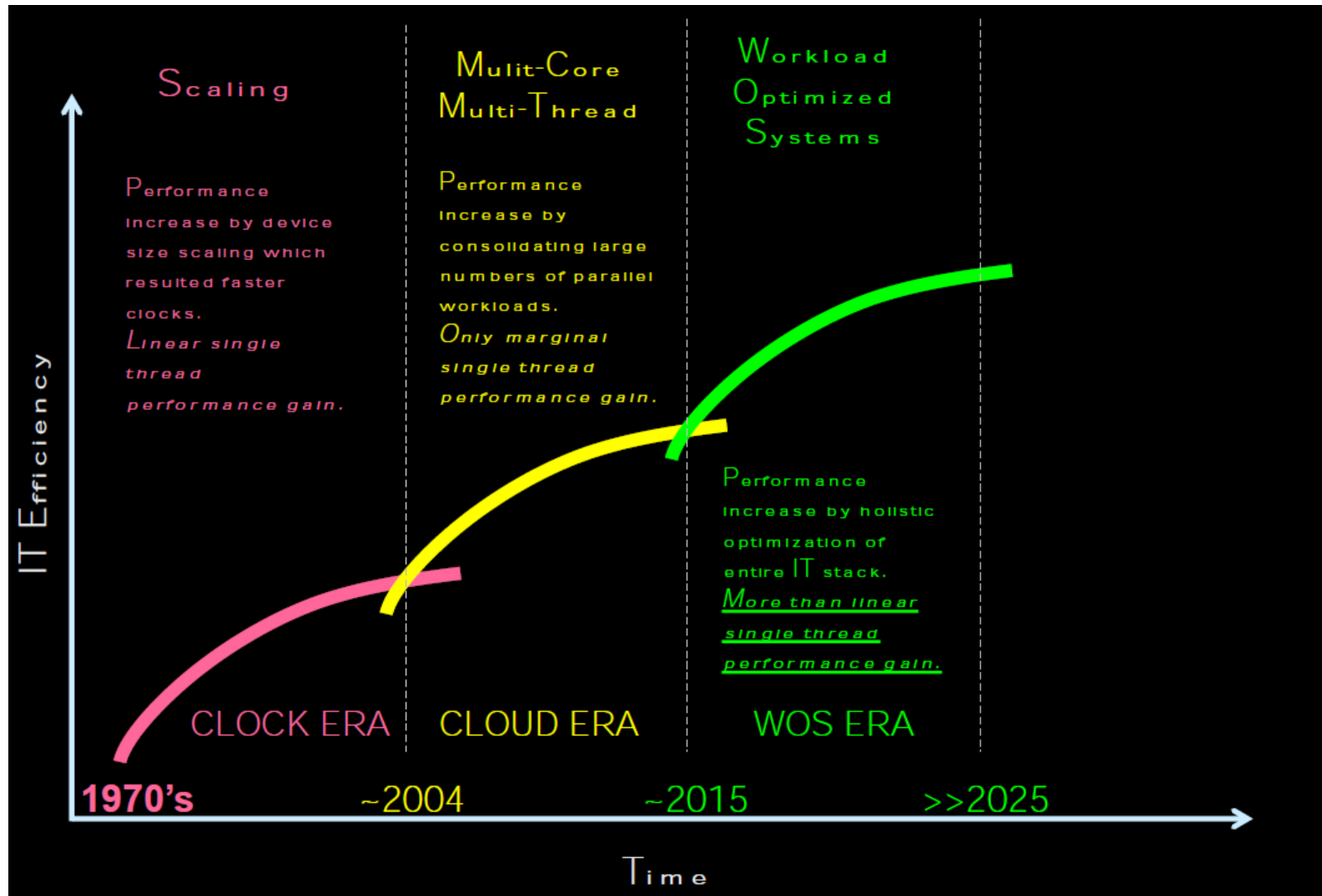


Agenda

- *POWER Future Technology*
 - *Next Generation Processor*
 - *Information about HighEnd System*
 - *PowerVM Management*
- *New PowerLinux Offering*

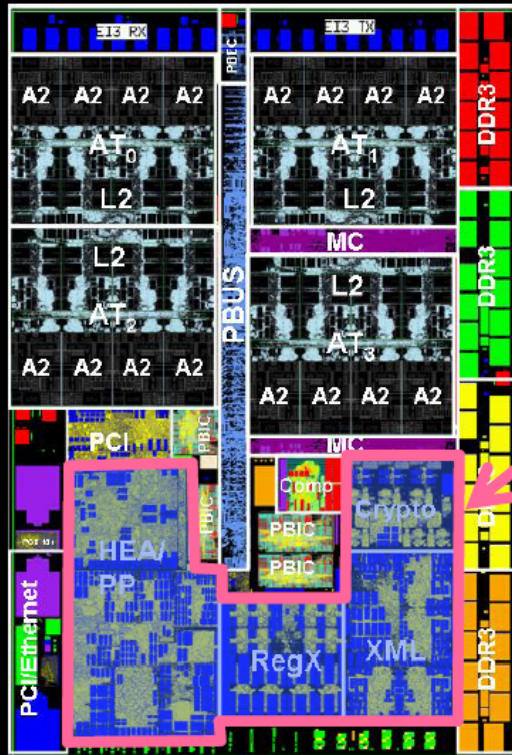


IBM vision : To the Workload Optimized Systems ...



Workload Optimized Systems Example

Network Computing with IBM WireSpeed Power Processor



Technology	IBM 45 _{nm} SOI
Core Frequency	2.3GHz @ 0.97V (Worst Case Process)
Chip Power (4-AT node)	65W @ 2.0GHz, 0.85V Max Single Chip
Chip Power (1-AT node)	20W @ 1.4GHz, 0.77V Min Single Chip
Transistor Count	1.43B
A2 Cores / Threads	16 / 64
Hardware Accelerators	Crypto, Compression, RegX, XML
Intelligent Network Interfaces	Host Ethernet Adapter/Processor 2 Modes: Endpoint & Network
Memory Bandwidth	2x DDR3 controllers 4 Channels @ 800-1600MHz
System I/O Bandwidth	4x 10G Ethernet, 2x PCI Gen2
Chip-to-Chip Bandwidth	3 Links, 20GB/s per link
Chip Scaling	4 Chip SMP

Optimized nodes with specialized network-speed processors
increase performance ~100 times (10'000%) => WOS clearly has a long-term potential.



POWER7+ Processors & Architecture

Faster Performance

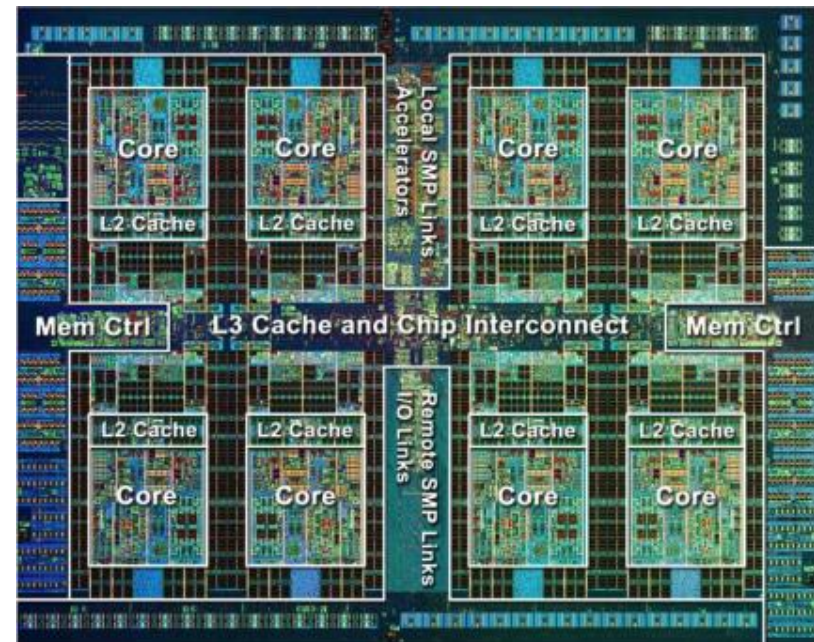
- Higher frequencies
- 80MB L3 Cache (10 MB per core)
- **HW Random number generator**
- **HW encryption accelerator (AIX)**
- Enhanced Single Precision Floating Point

Increased Efficiency and Flexibility

- **HW Memory Expansion accelerator**
- More performance per watt
- Enhanced energy / power gating
- **20 Virtual Machines per core**

Better Availability RAS

- Self-healing capability for L3 Cache functions
- Processor re-initialization



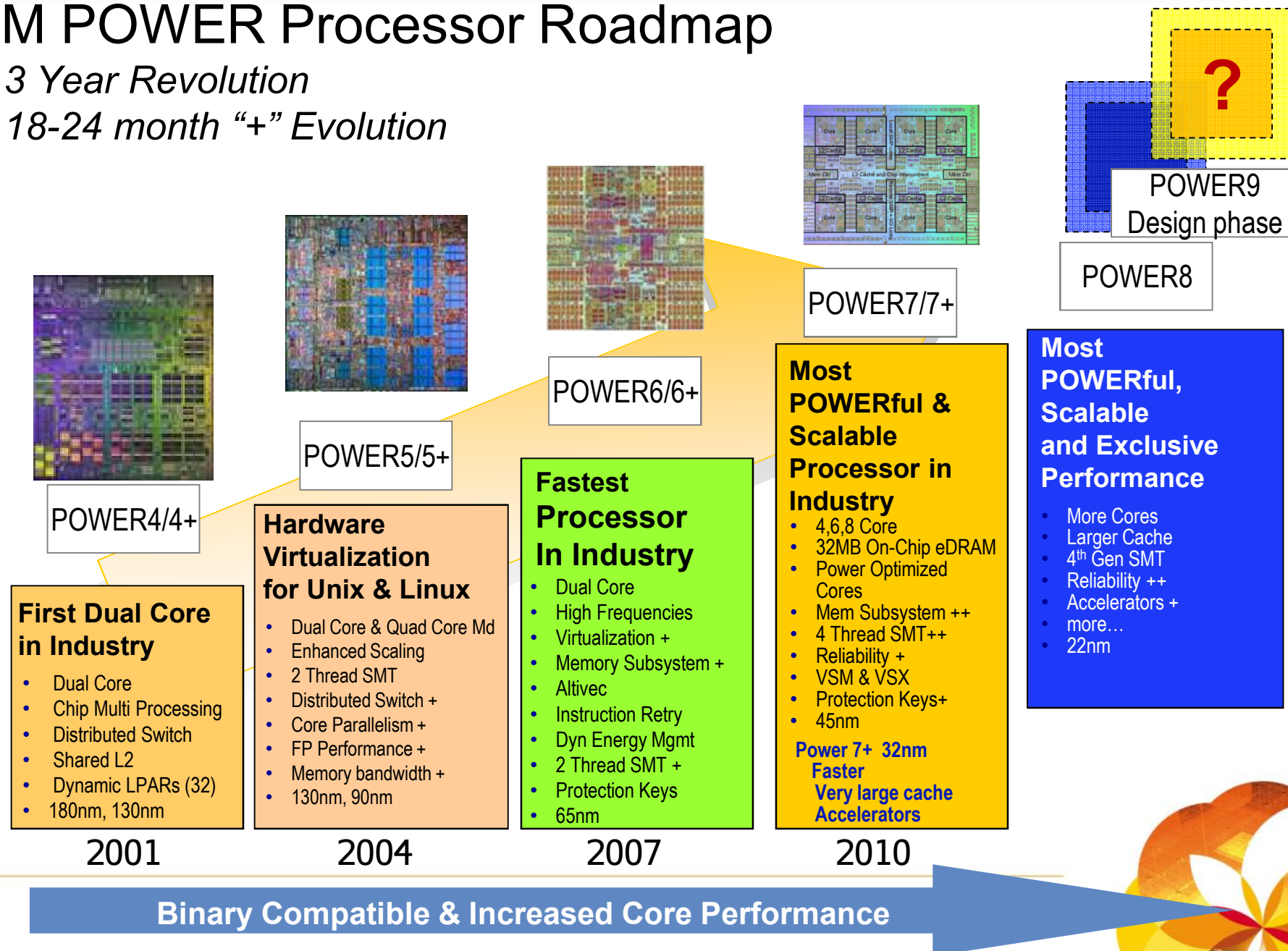
POWER7+
32 nm



IBM POWER Processor Roadmap

~ 3 Year Revolution

~ 18-24 month "+" Evolution



POWER8 Processor

Technology

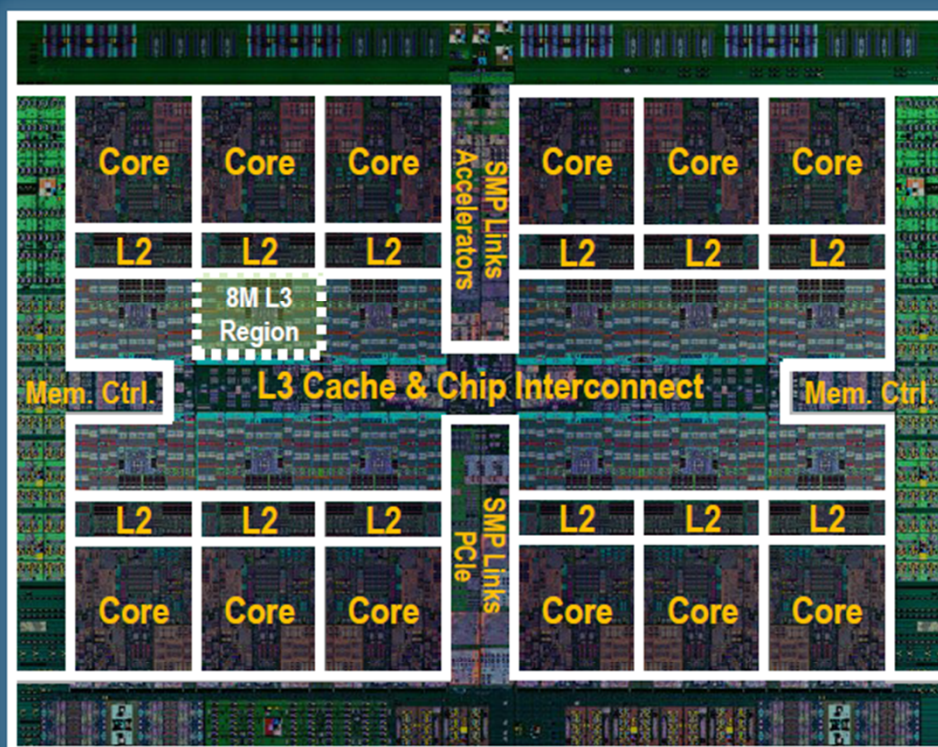
- 22nm SOI, eDRAM, 15 ML 650mm²

Cores

- 12 cores (SMT8)
- 8 dispatch, 10 issue, 16 exec pipe
- 2X internal data flows/queues
- Enhanced prefetching
- 64K data cache, 32K instruction cache

Accelerators

- Crypto & memory expansion
- Transactional Memory
- VMM assist
- Data Move / VM Mobility



Energy Management

- On-chip Power Management Micro-controller
- Integrated Per-core VRM
- Critical Path Monitors

Caches

- 512 KB SRAM L2 / core
- 96 MB eDRAM shared L3
- Up to 128 MB eDRAM L4 (off-chip)

Memory

- Up to 230 GB/s sustained bandwidth

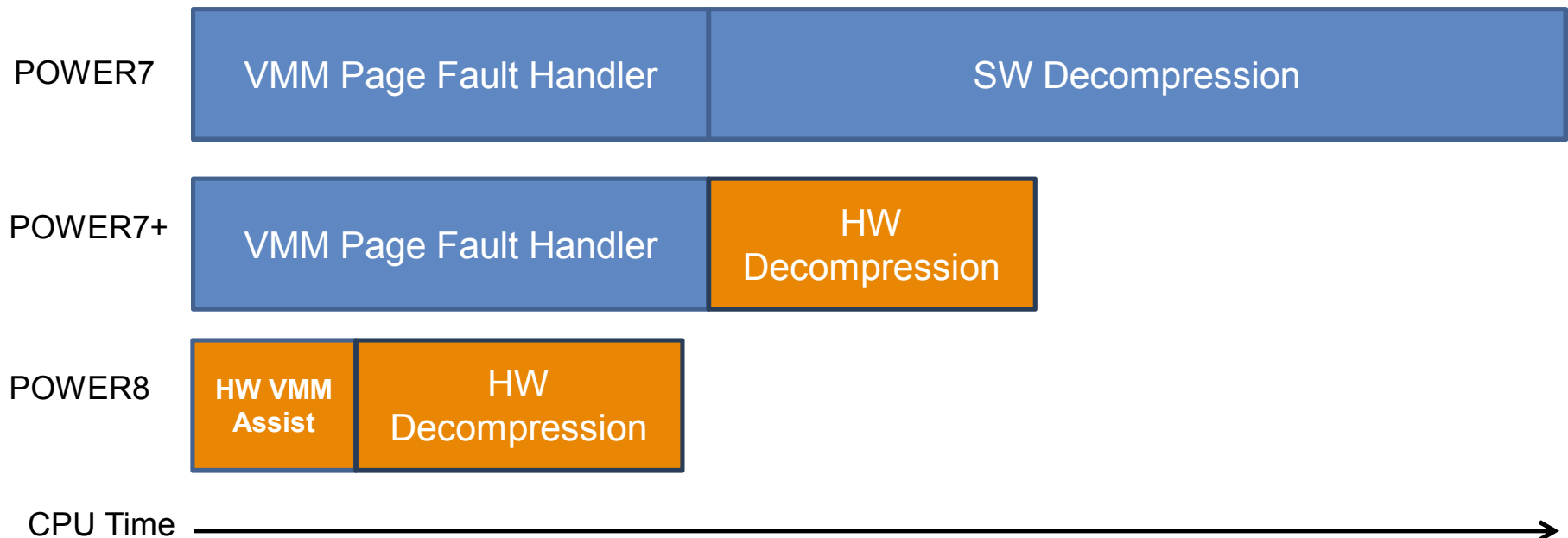
Bus Interfaces

- Durable open memory attach interface
- Integrated PCIe Gen3
- SMP Interconnect
- CAPI (Coherent Accelerator Processor Interface)

POWER8 - AME Enhanced



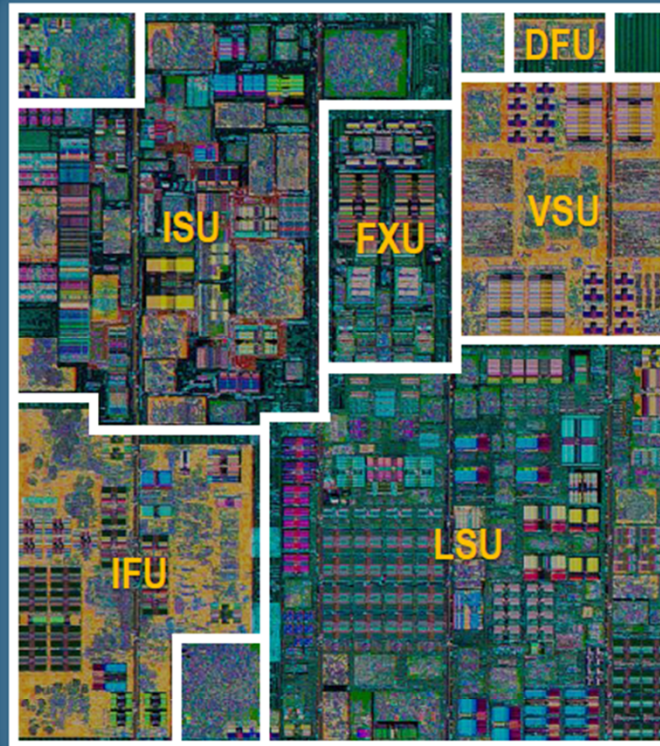
- POWER7+ embedded HW compression accelerator improves by up to 2.1x decompression time
- POWER8 will accelerate VMM with Hardware. This will improve AME and LPM performance.



POWER8 Core

Execution Improvement vs. POWER7

- SMT4 → SMT8
- 8 dispatch
- 10 issue
- 16 execution pipes:
 - 2 FXU, 2 LSU, 2 LU, 4 FPU, 2 VMX, 1 Crypto, 1 DFU, 1 CR, 1 BR
- Larger Issue queues (4 x 16-entry)
- Larger global completion, Load/Store reorder
- Improved branch prediction
- Improved unaligned storage access



Larger Caching Structures vs. POWER7

- 2x L1 data cache (64 KB)
- 2x outstanding data cache misses
- 4x translation Cache

Wider Load/Store

- 32B → 64B L2 to L1 data bus
- 2x data cache to execution dataflow

Enhanced Prefetch

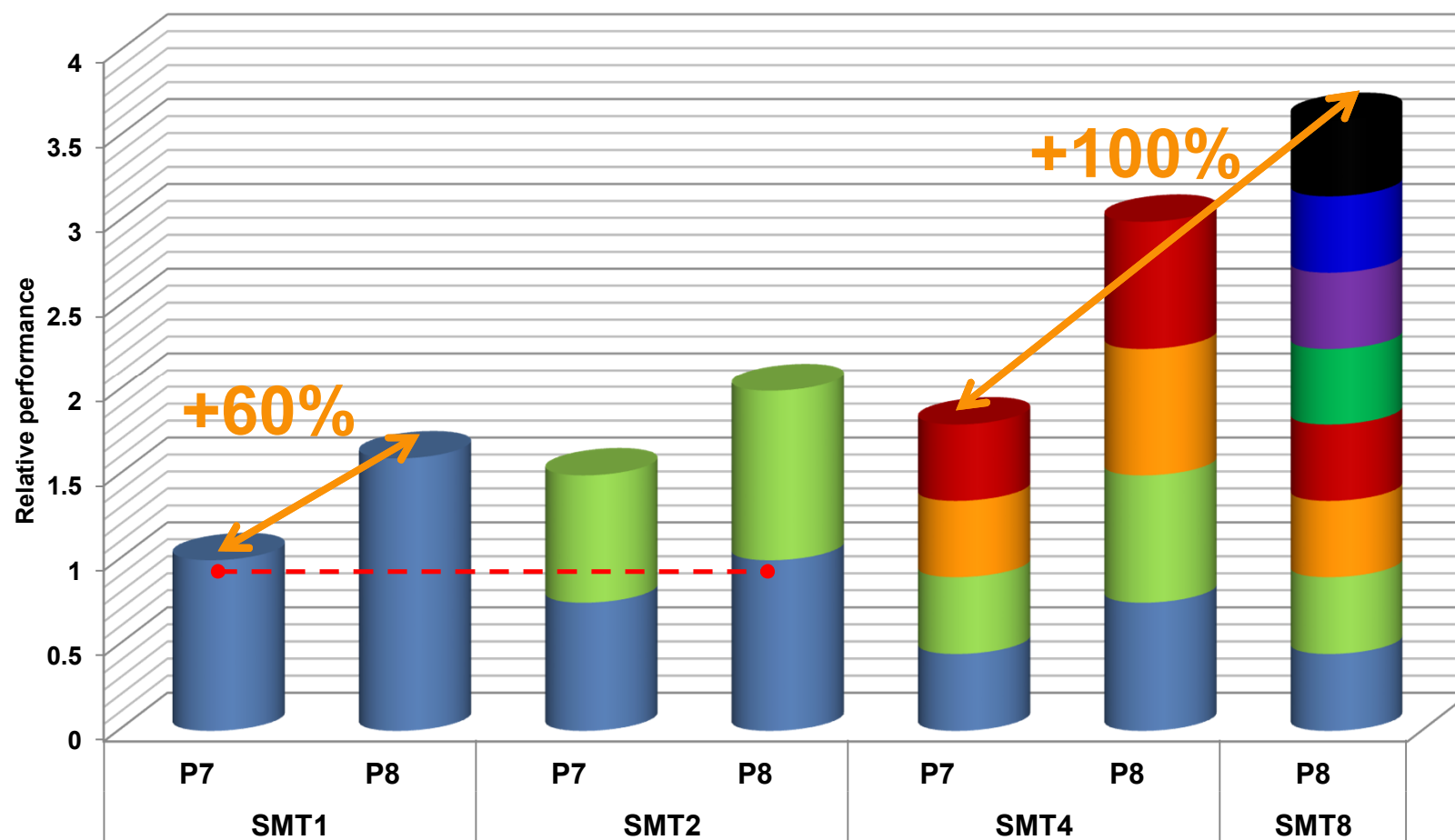
- Instruction speculation awareness
- Data prefetch depth awareness
- Adaptive bandwidth awareness
- Topology awareness

Core Performance vs. POWER7

~1.6x Single Thread

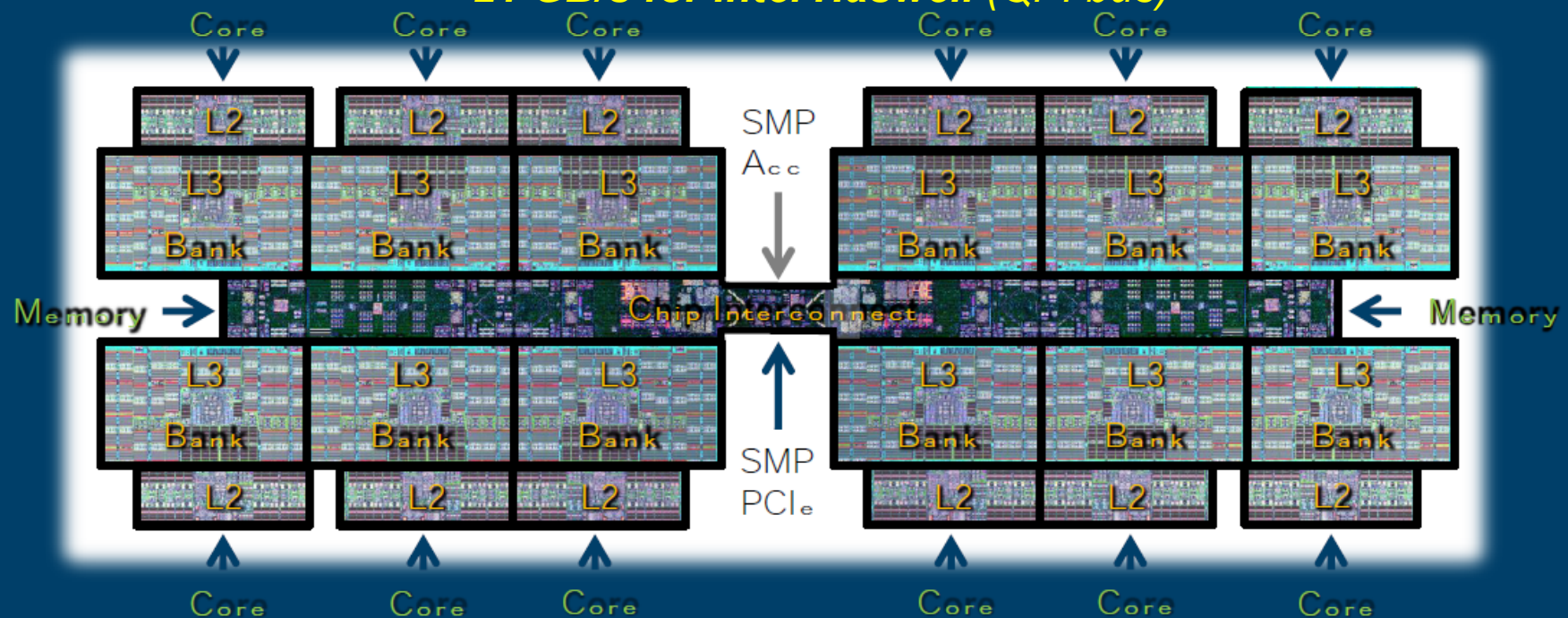
~2x Max SMT

POWER7+ vs POWER8 – SMT performance



POWER8 On Chip Caches

- L2: 512 KB 8 way per core *X2 Intel Ivy Bridge & Haswell*
- L3: 96 MB (12 x 8 MB 8 way Bank) *8MB shared for Intel Ivy Bridge & Haswell*
- “NUCA” Cache policy (Non-Uniform Cache Architecture)
 - Scalable bandwidth and latency
 - Migrate “hot” lines to local L2, then local L3 (replicate L2 contained footprint)
- Chip Interconnect: 150 GB/sec x 12 segments per direction = 3.6 TB/sec
~21 GB/s for Intel Haswell (QPI bus)



Cache Bandwidths

Core



256

64

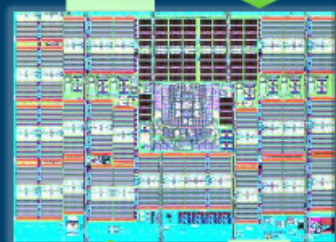
L2



128

128

L3

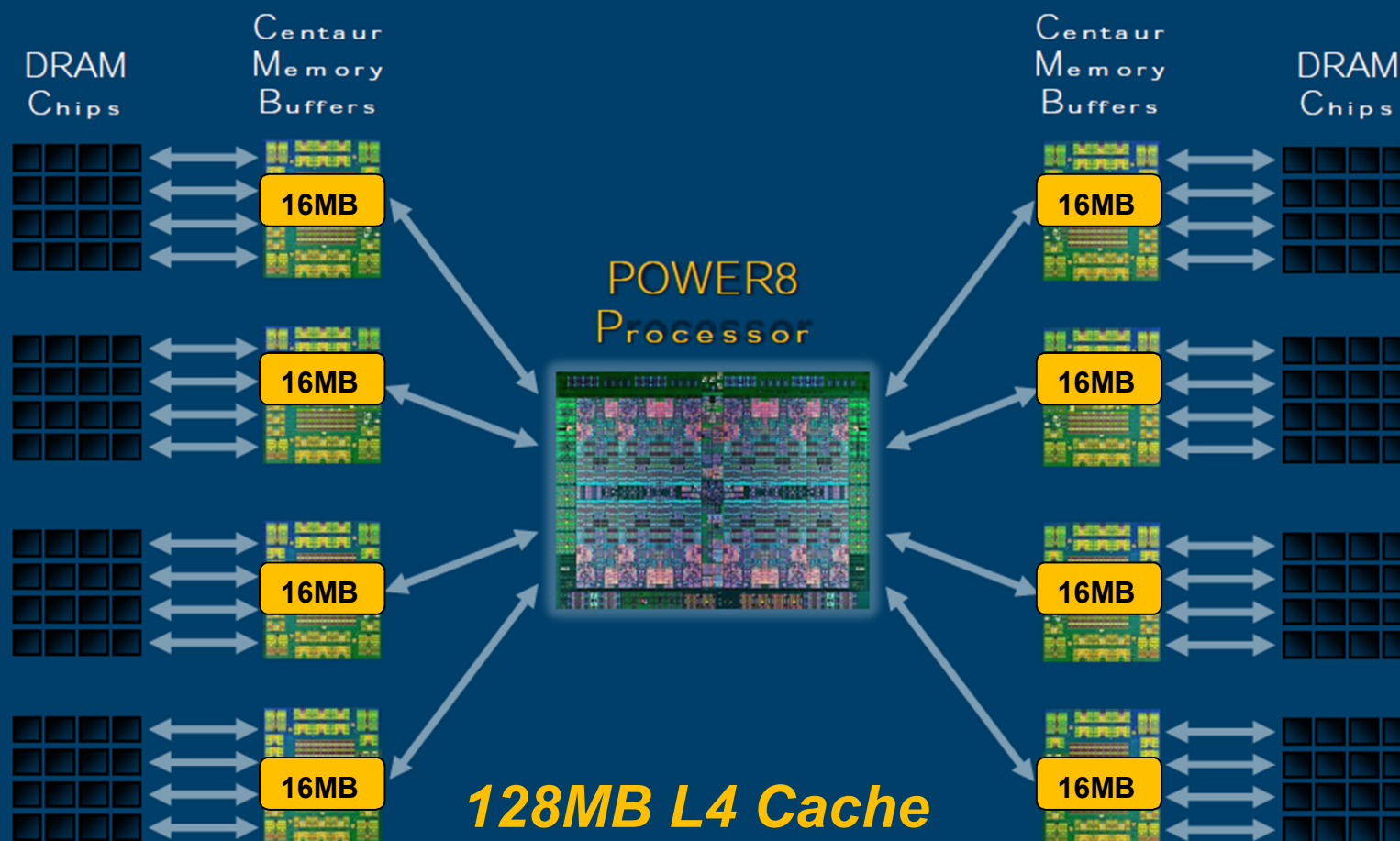


128

64

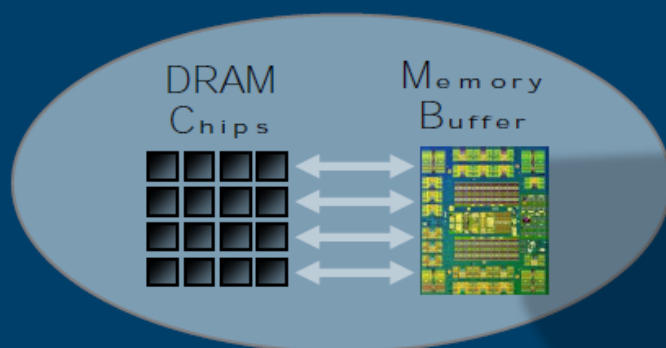
- ➔ GB/sec shown assuming 4 GHz
 - Product frequency will vary based on model type
- ➔ Across 12 core chip
 - 4 TB/sec L2 BW
 - 3 TB/sec L3 BW

POWER8 Memory Organization



- ➔ Up to 8 high speed channels, each running up to 9.6 Gb/s for up to 230 GB/s sustained
- ➔ Up to 32 total DDR ports yielding 410 GB/s peak at the DRAM
- ➔ Up to 1 TB memory capacity per fully configured processor socket

POWER8 Memory Buffer Chip ...with 16MB of Cache...



Intelligence Moved into Memory

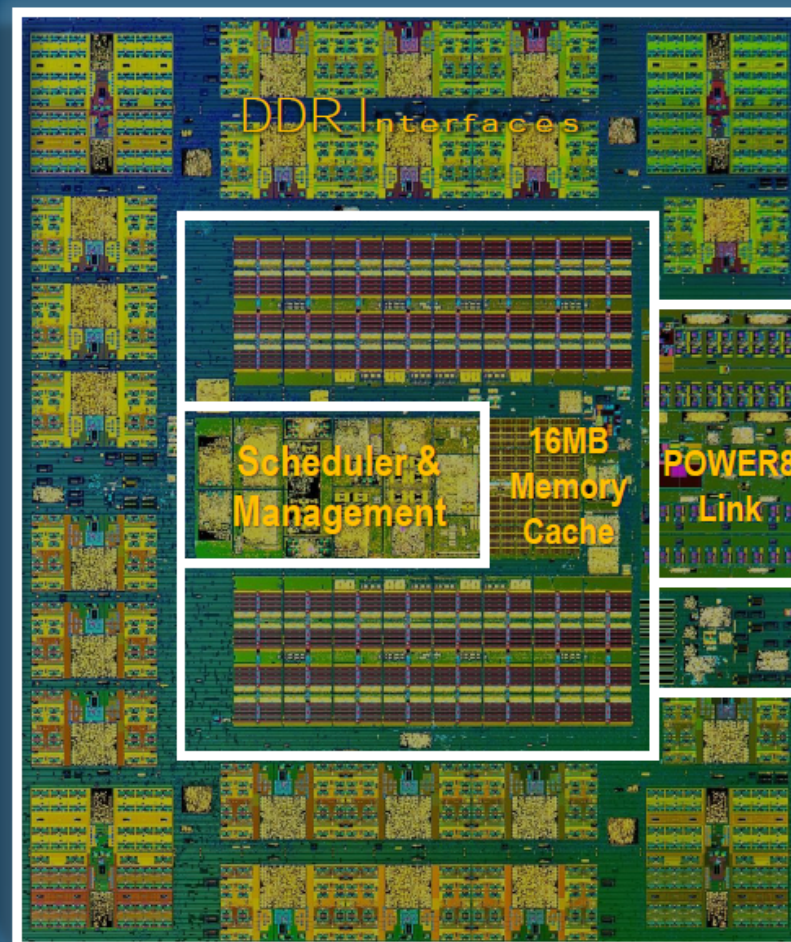
- Scheduling logic, caching structures
- Energy Mgmt, RAS decision point
 - Formerly on Processor
 - Moved to Memory Buffer

Processor Interface

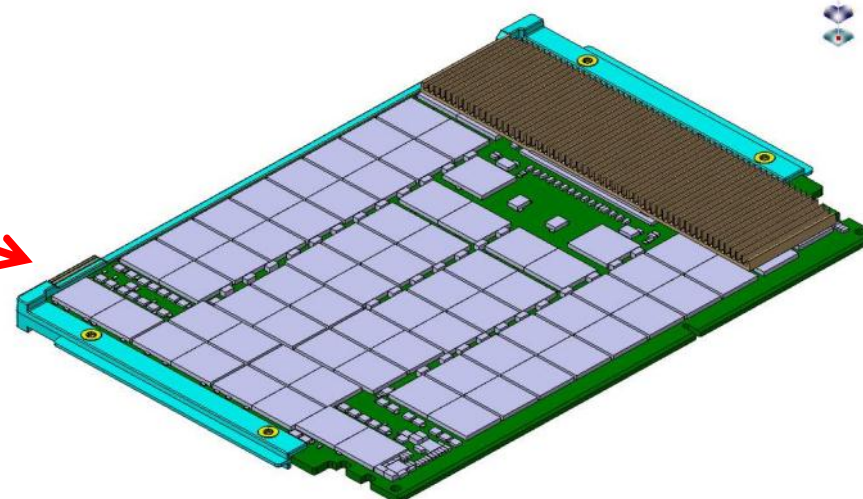
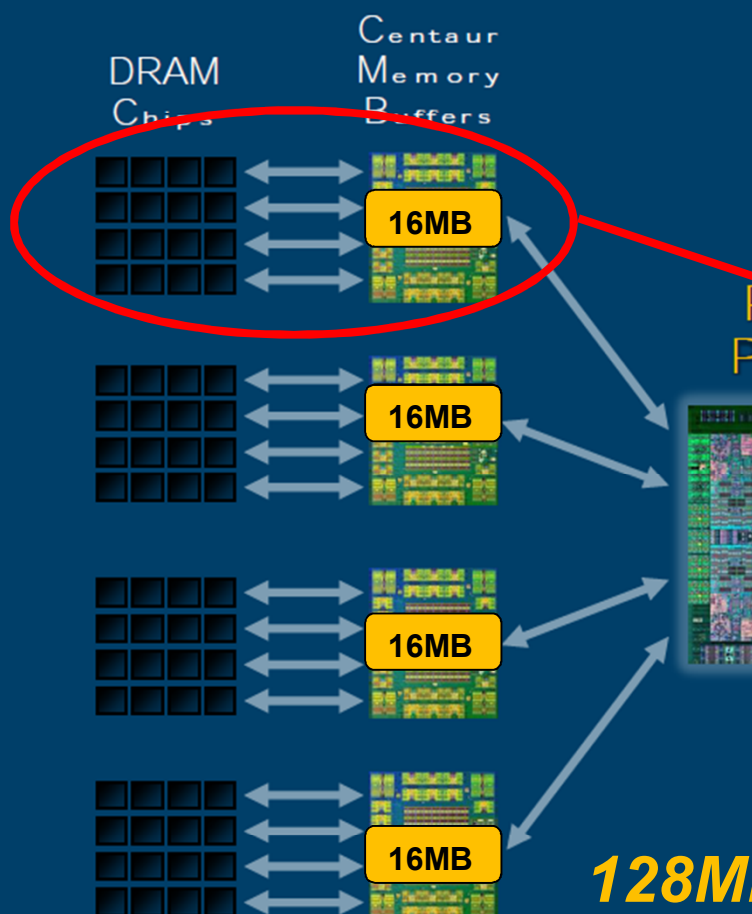
- 9.6 GB/s high speed interface
- More robust RAS
- “On-the-fly” lane isolation/repair
- Extensible for innovation build-out

Performance Value

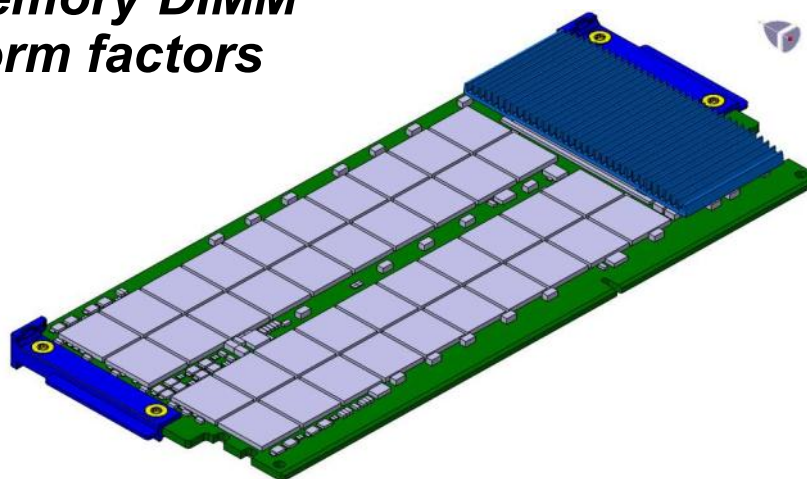
- End-to-end fastpath and data retry (latency)
- Cache → latency/bandwidth, partial updates
- Cache → write scheduling, prefetch, energy
- 22nm SOI for optimal performance / energy
- 15 metal levels (latency, bandwidth)



POWER8 Memory Organization



**Memory DIMM
Form factors**

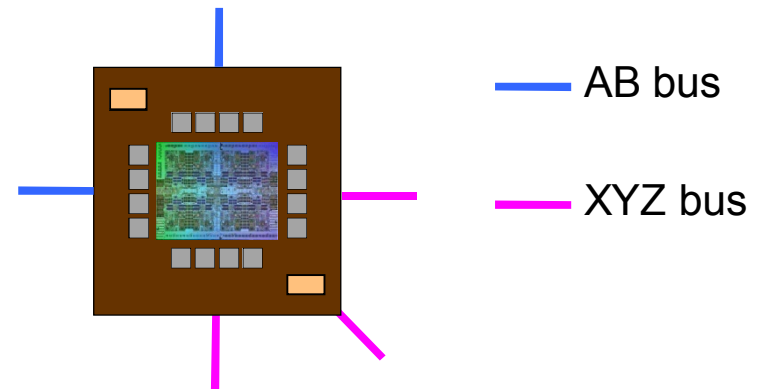


- ➔ Up to 8 high speed channels, each with 4 memory buffers
- ➔ Up to 32 total DDR ports yielding 41GB/s bandwidth
- ➔ Up to 1 TB memory capacity per fully configured processor socket

POWER: Socket connection

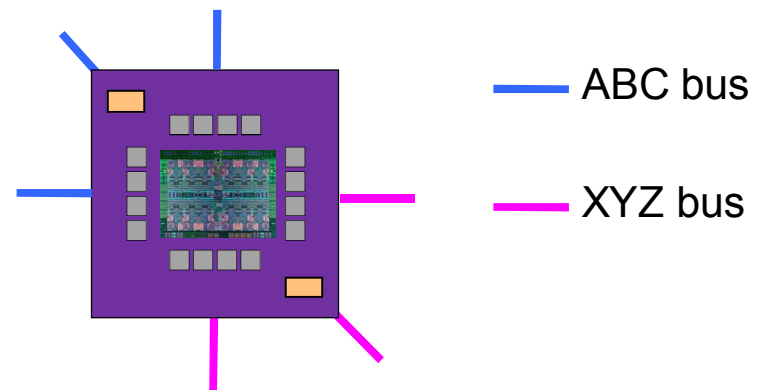
POWER7 Chip

- 3 intra nodes connection per chip
 - 2 inter nodes connection per chip
 - Up to 8 nodes
- => **HighEnd : Max 3 hop interconnect**

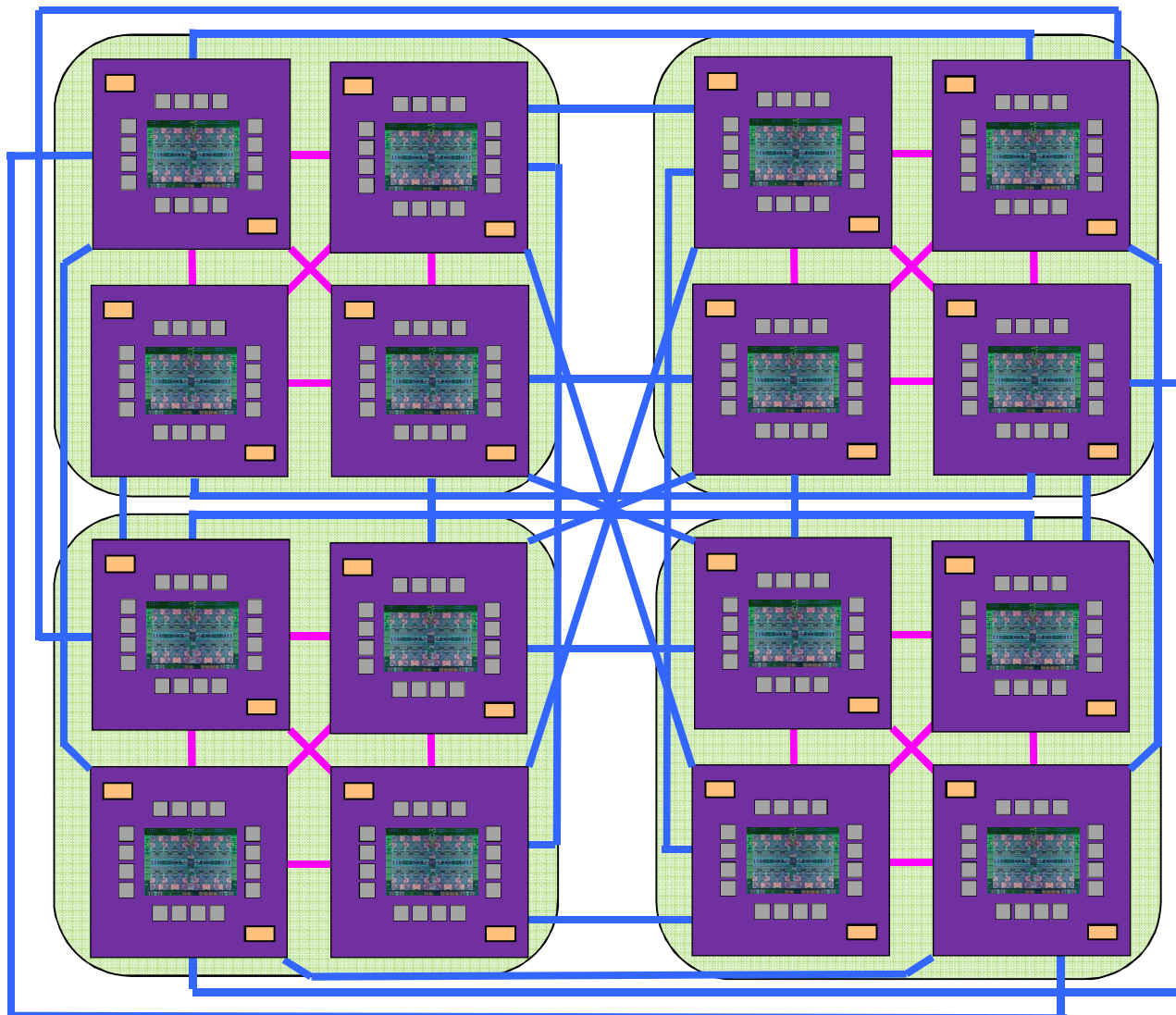


POWER8 Chip

- 3 intra nodes connection per chip
 - 3 inter nodes connection per chip
 - UP to 4 nodes
- => **HighEnd : Max 2 hop interconnect**

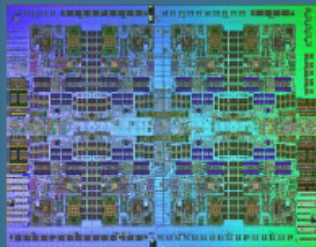


POWER8 : High End socket/node connection



POWER8 Integrated PCIe Gen 3

POWER7

GX
BusI/O
Bridge

PCIe G2

PCI
Device

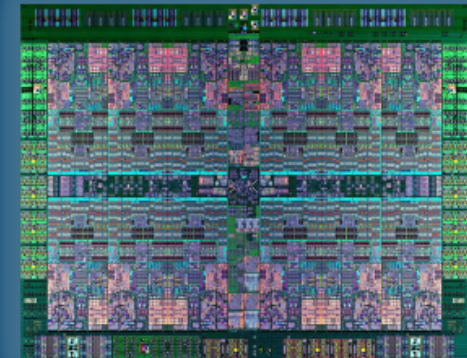
Native PCIe Gen 3 Support

- Direct processor integration
- Replaces proprietary GX/Bridge
- Low latency
- Gen3 x16 bandwidth (16 Gb/s)

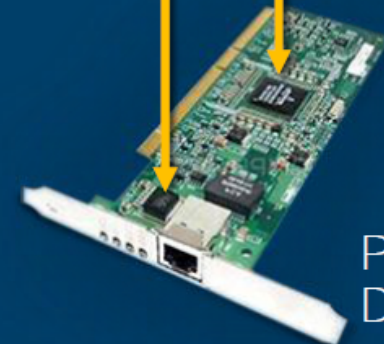
Transport Layer for CAPI Protocol

- Coherently Attach Devices connect to processor via PCIe
- Protocol encapsulated in PCIe

POWER8



PCIe G3

PCI
Device

POWER8 CAPI

Coherent Accelerator Processor Interface

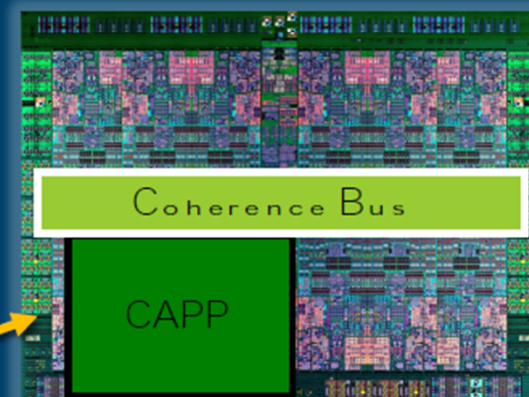
Virtual Addressing

- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead

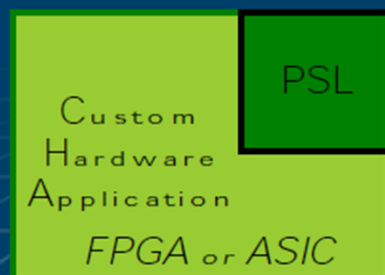
Hardware Managed Cache Coherence

- Enables the accelerator to participate in “Locks” as a normal thread
- Lowers Latency over IO communication model

POWER8



PCIe Gen 3

Transport for encapsulated messages

Customizable Hardware Application Accelerator

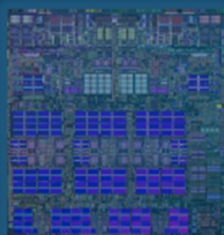
- Specific system SW, middleware, or user application
- Written to durable interface provided by PSL

Processor Service Layer (PSL)

- Present robust, durable interfaces to applications
- Offload complexity / content from CAPP

POWER8 Innovation

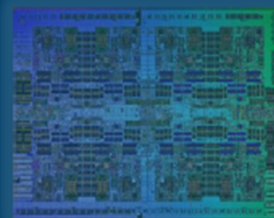
POWER5
2004



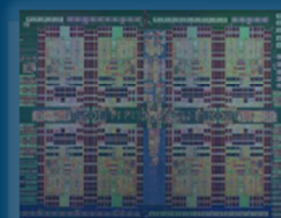
POWER6
2007



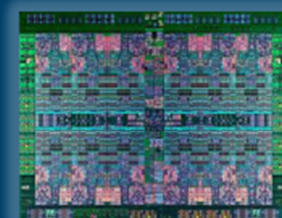
POWER7
2010



POWER7+
2012



POWER8



Technology

Compute

Cores
Threads

Caching

On-chip
Off-chip

Bandwidth

Sust. Mem.
Peak I/O

130_nm SOI

2

SMT2

1.9MB

36MB

15GB/s

6GB/s

65_nm SOI

2

SMT2

8MB

32MB

30GB/s

20GB/s

45_nm SOI
eDRAM

8

SMT4

2 + 32MB

None

100GB/s

40GB/s

32_nm SOI
eDRAM

8

SMT4

2 + 80MB

None

100GB/s

40GB/s

22_nm SOI
eDRAM

12

SMT8

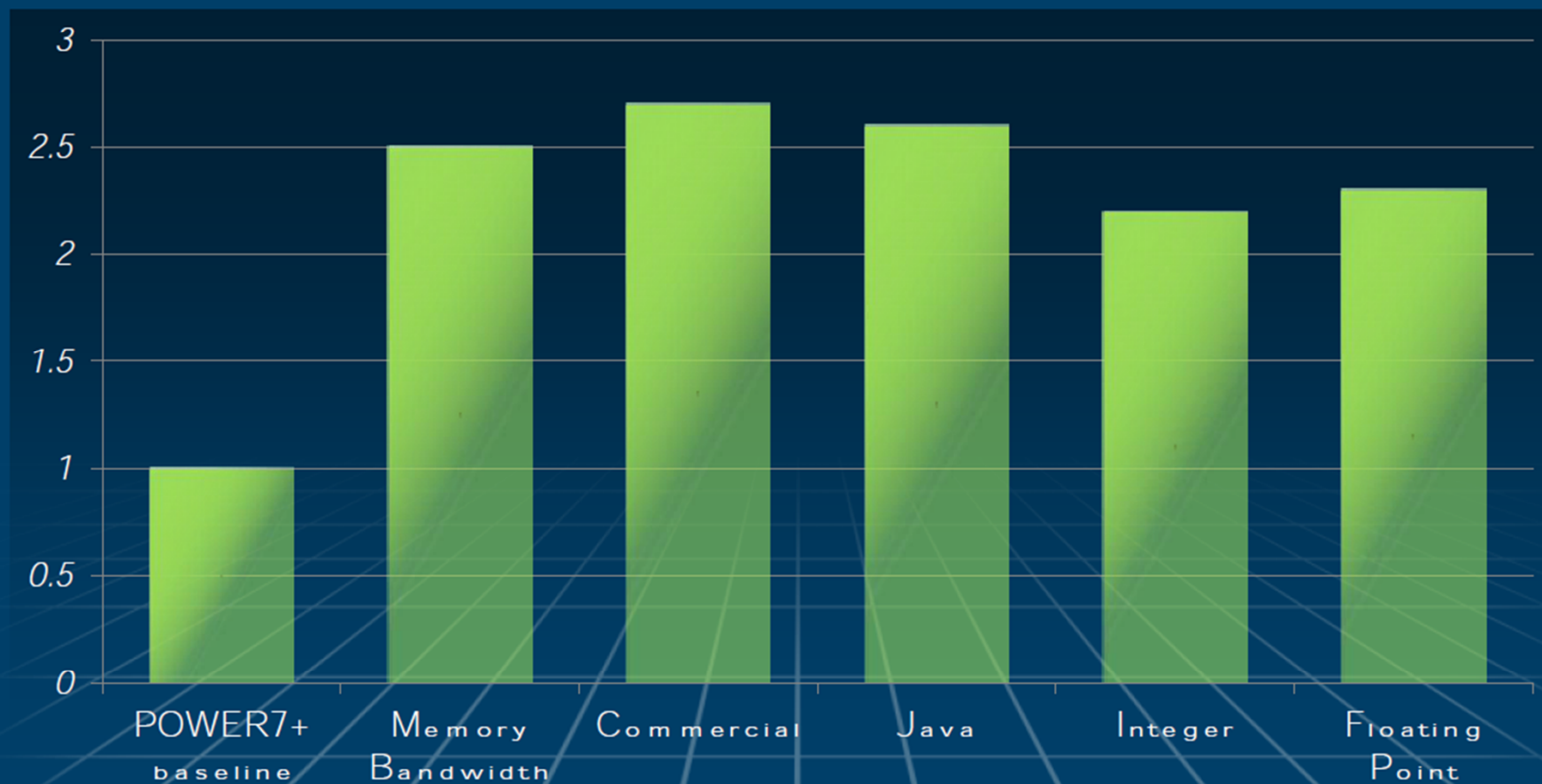
6 + 96MB

128MB

230GB/s

96GB/s

Socket Performance



POWER8 Enabling: ...Big Data, Analytics, Cognitive Computing...

POWER8 Differentiation for Analytics

- Massive capacity and bandwidth to memory and IO
- Large caches with massive bandwidth
- Strong Single thread
- SMT8, Many threads to hide memory latency
 - Graph traversals
 - Transactional memory enables efficient thread scaling

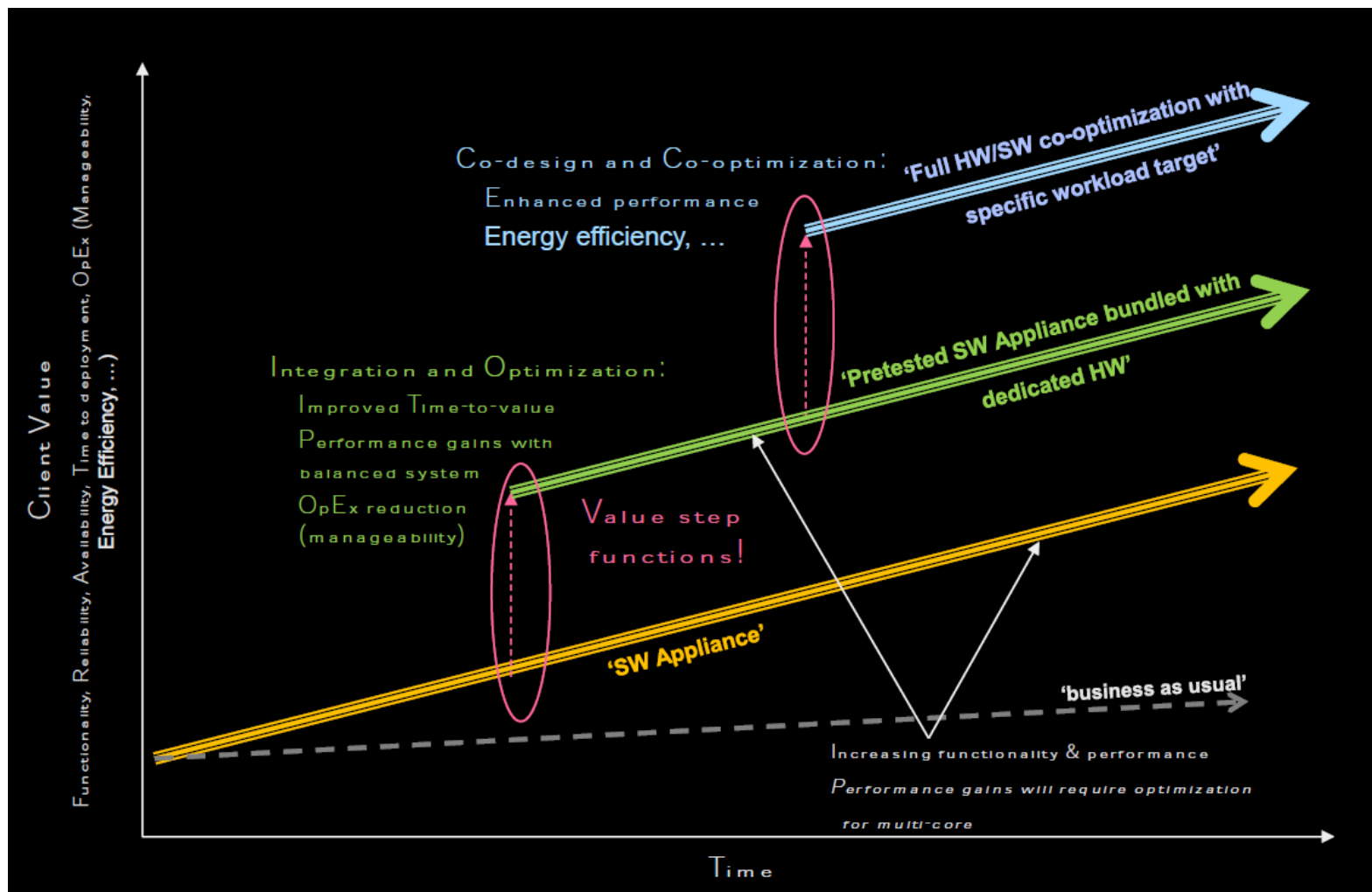
CAPI Accelerators

- Enables heterogeneous compute (GPU, FPGA, etc.)

Synergy with IBM Software, Driving Optimization Across the Stack

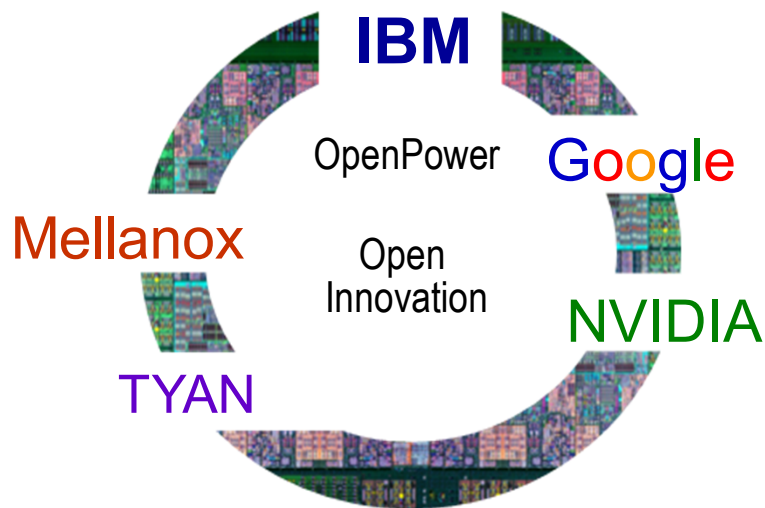


Client Value Step Functions through Workload Optimization



POWER8... Giving ecosystem partners a license to innovate...

OpenPOWER will enable hyper-scale cloud data centers to rethink their approach to technology.



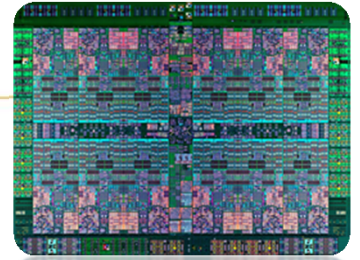
Member companies will use **POWER** for custom open servers and components for Linux based cloud data centers.

First time, **OpenPOWER** ecosystem partners can optimize the interactions of server building blocks – microprocessors, networking, I/O & other components – to tune performance.



POWER8 Highlights

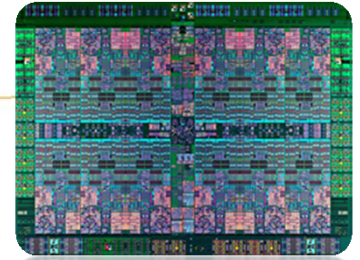
PERFORMANCE



The Register: *“it most certainly does belong in a **badass** server, and Power8 is by far one of the most elegant chips that Big Blue has ever created”*

- **Huge performance improvement:**
 - **1.5X** to **1.7X** thread-level improvement*
 - **2X** core improvement*
 - **3X** socket improvement*
- **Compared with POWER7+**
 - Commercial **2.5X*** and Java **2.6X***
 - Integer **2.2X*** and Floating Point **2.3X***
- **Coherent Accelerators (CAPI) – memory-space addressable**
- **SMP scaling**
 - 16 sockets, 192 cores
 - Lower latency, high speed





POWER8 Highlights

MEMORY and BANDWIDTH

Linley Group microprocessor report: “The Power8 specs are mind boggling. . . IBM’s newest server processor will smash existing performance records, particularly for memory-intensive applications”



- **Caching Structure**
 - L1 to L4 cache with Non-Uniform Cache Architecture
 - **4 TB/s** L2 bandwidth* per chip (4GHz 12core)
 - **3 TB/s** L3 bandwidth* per chip (4GHz 12core)
- **Memory Subsystem**
 - **230 GB/s** sustained* bandwidth per chip
 - **410 GB/s** bandwidth* at DRAM level per chip
 - **1 TB** memory per socket (e.g. 4sockets = 4 TB)
 - Transactional Memory

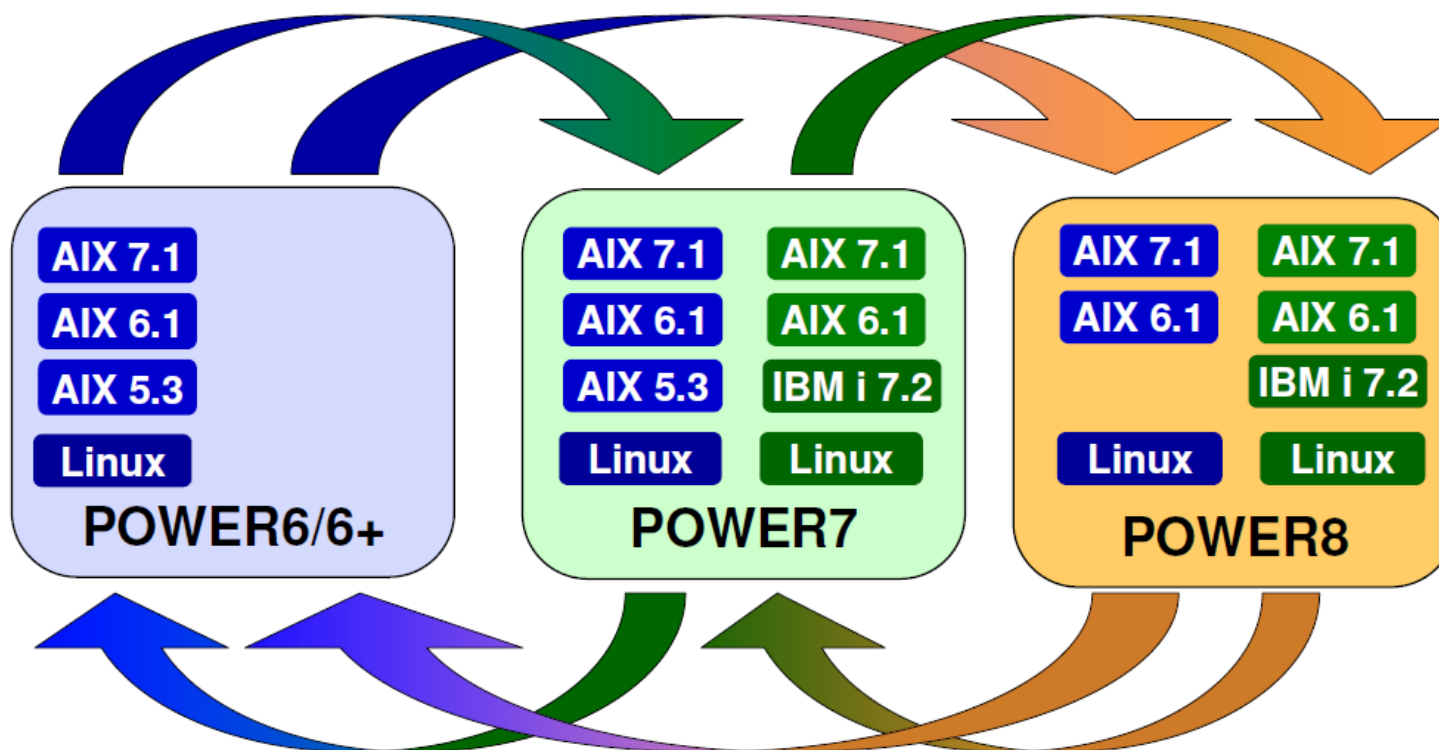


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POWER6 / POWER7 / POWER8 Partition Mobility



Leverage POWER6 / POWER7 Compatibility Modes

LPAR Migrate between POWER6 / POWER7 / POWER8 Servers

Can not move POWER8 Mode partitions to POWER6 or POWER7 systems.



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BONUS Break : 5min Technology

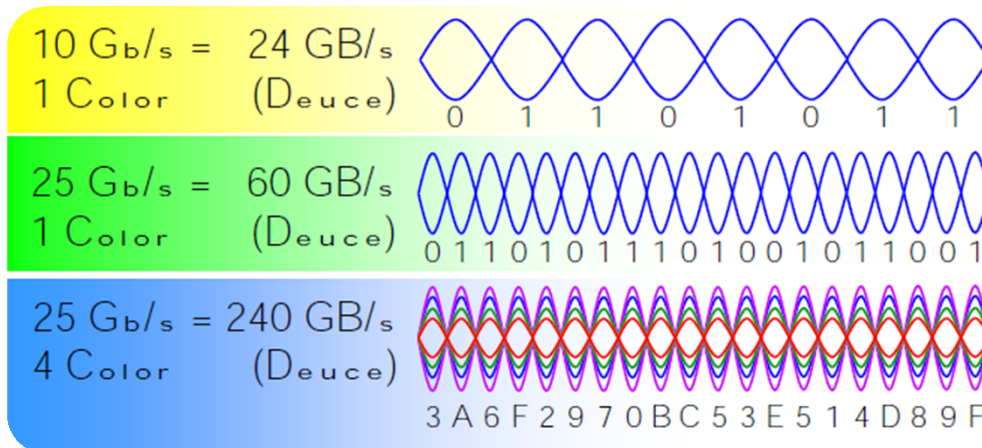
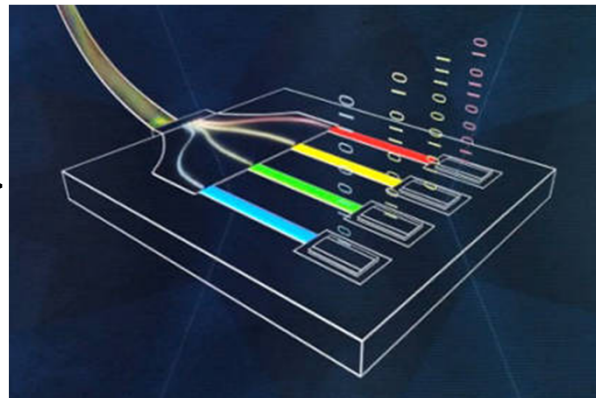
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Optical Interconnects – Silicon Photonic

Disruptive Optics Evolution and
Silicon Photonics

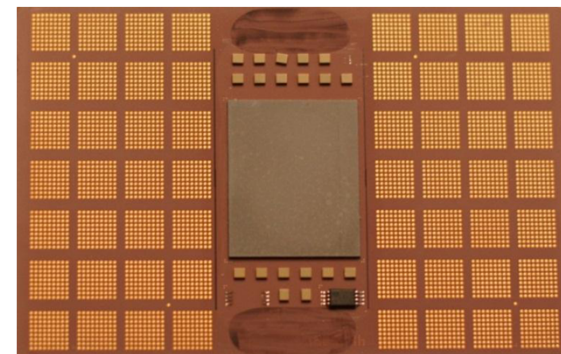
*Silicon Photonics,
Multi-wavelength, =>
25 Gb/s Optics*



POWER7 775 HPC system

High density IO off module
optical transceivers

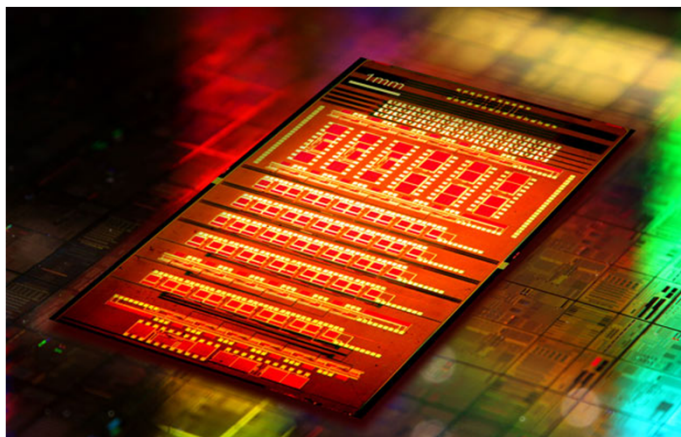
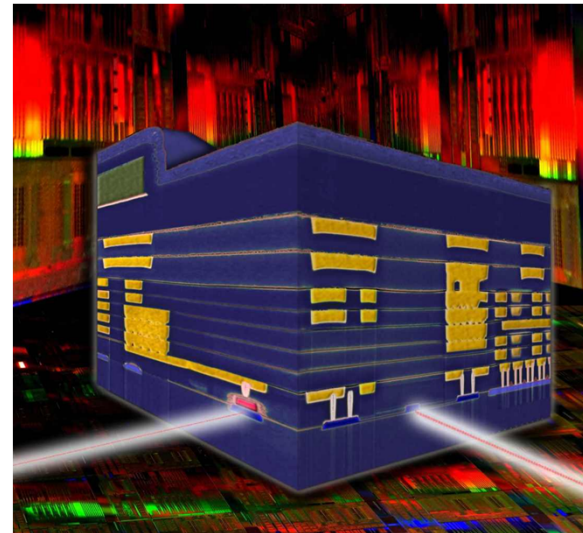
- Physical escape density
- P7 775 HPC network chip
shown below
- Tx : 12 x 10Gb/s
- Rx : 12 x 10Gb/s



IBM - Silicon Integrated Nanophotonics

An IBM 90nm Silicon Integrated Nanophotonics technology is capable of integrating a photodetector (red feature on the left side of the cube) and modulator (blue feature on the right side of the cube) fabricated side-by-side with silicon transistors (red sparks on the far right of the cube).

Silicon Nanophotonics circuits and silicon transistors are interconnected with nine levels of yellow metal wires.



IBM Silicon Nanophotonics technology is capable of integrating optical and electrical circuits side-by-side on the same chip.

IBM develops the **TINIEST nanophotonic switch** able to connect Tb/s network. This technology can be used for chips interconnection in next generation systems.

Sources:

http://researcher.watson.ibm.com/researcher/view_project.php?id=2757

http://news.cnet.com/8301-30685_3-20024223-264.html



3D Stacking

Today's 2D designs :

Larger structures introduce longer physical distances creating a design conflict :

- Increase latency
- Need more power

3D designs :

Many-levels of chips with low power and latency communication

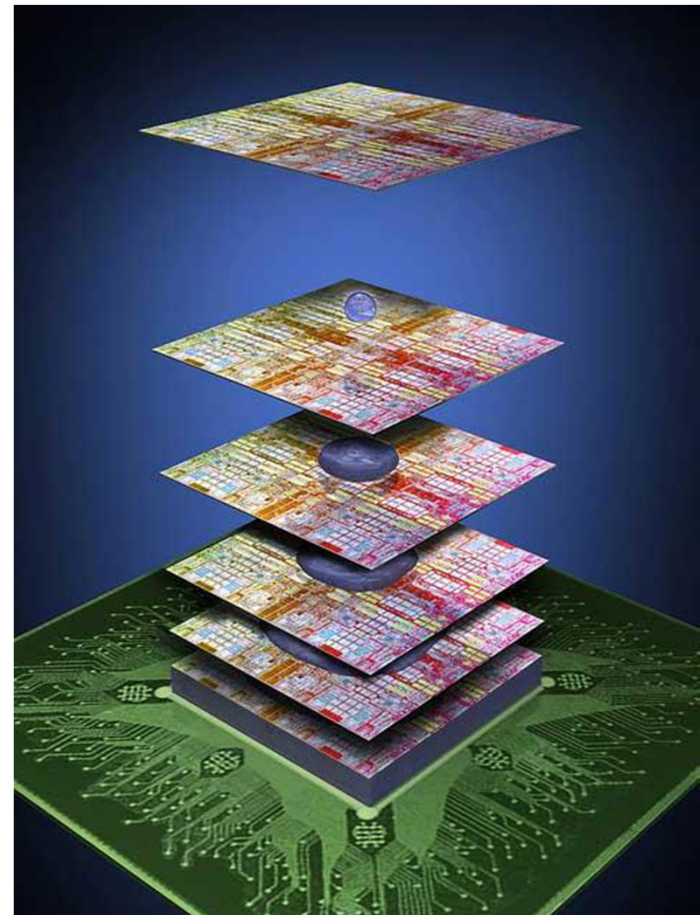
- Enables larger caches stacked below the CPU
- Enables larger chips with good yield

1st generation : Pull external interface logic and voltage regulation into lower layer

2nd generation : Add an L3 cache layer

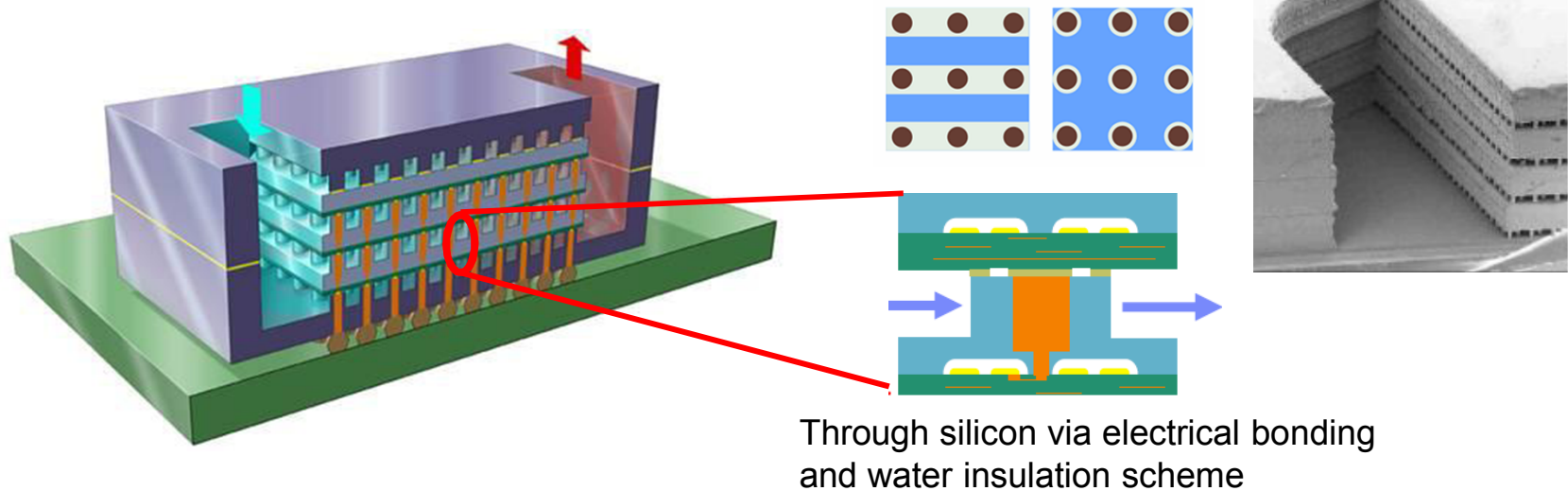
3rd generation : Move L2 cache and large second level core centric structures (TLB, Predictors)

4th generation : Two layer CPU, execution units on top, L1 caches below

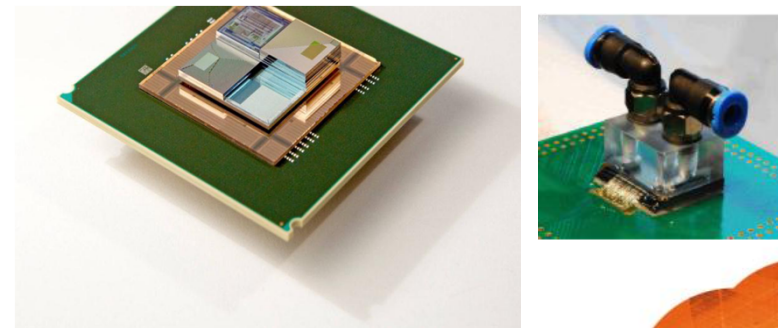


Scalable Heat Removal by Interlayer Cooling

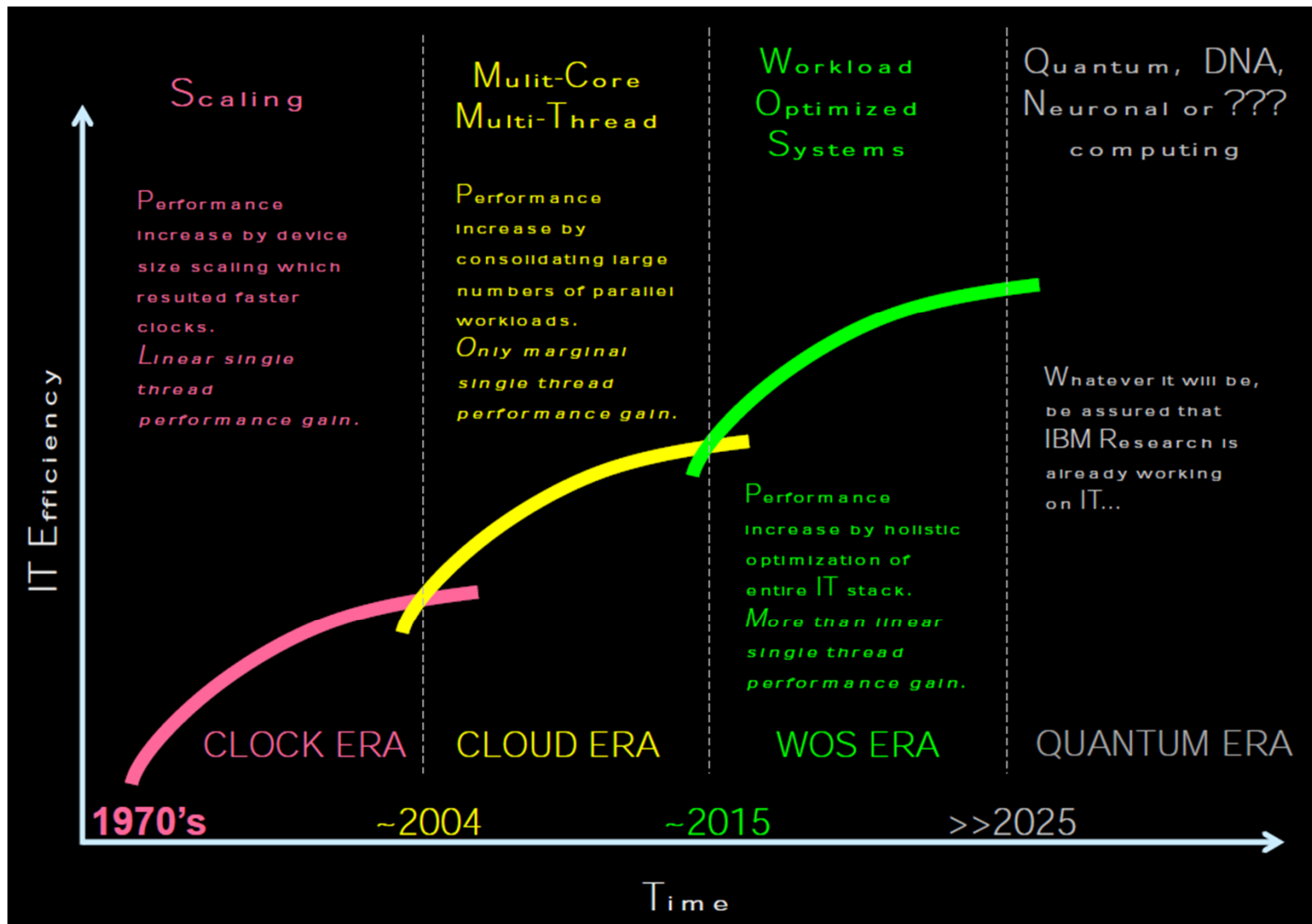
- 3D integration requires interlayer cooling for stacked logic chips
- Bonding scheme to isolate electrical interconnects from coolant



- A large fraction of energy in computers is spent for data transport
- Shrinking computers saves energy



IT Performance Evolution: Outlook to the future



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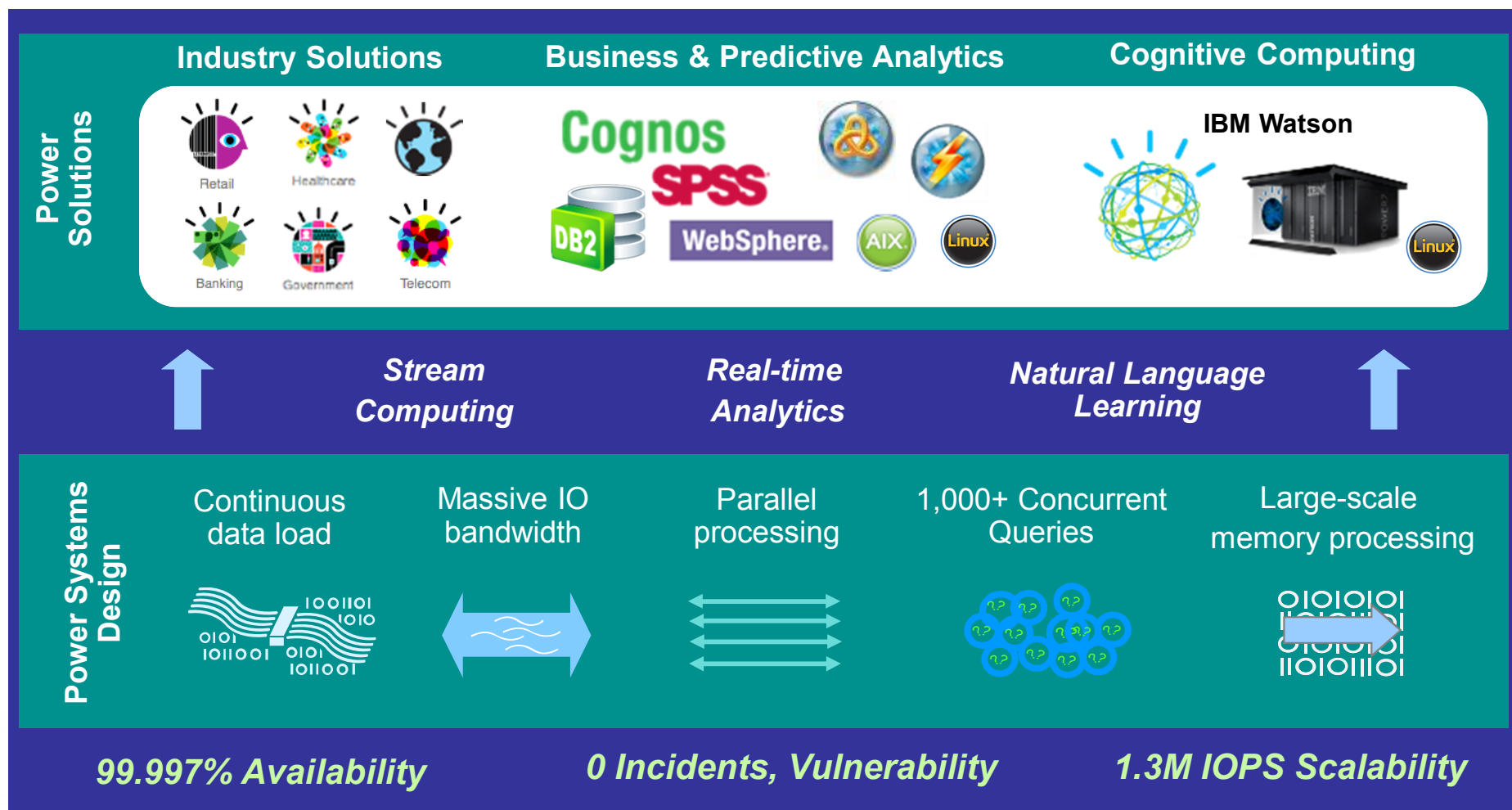


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Power enable next gen applications & cognitive computing



Open & flexible infrastructure - Available on premise or through the Cloud



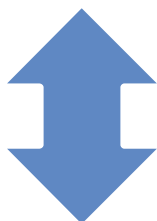
Expanding POWER into Big Data, Analytics, Cloud, Linux

POWER recognized leader for

- Business Applications – ERP, OLTP, Enterprise Web Applications
- Data Warehousing/Minig/Analitics
- Data Store
- Workload Consolidation
- Investment Protection

Expansion Focus

- Big Data & Analitics
- New Industry Solutions
- Cloud Computing
- Open Source
- Cognitive Computing / IBM Watson



High Performance	Scalability	DataCapabilities	Security
Efficiency	Reliability & Availability	Advanced Virtualization	
Industry Affiliation	Mature & Growth Market	Large Scale Adoption	



New PowerLinux Offering



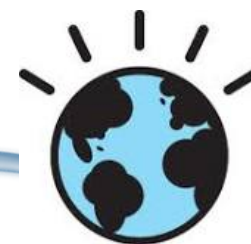
L'open source est un facteur important d'innovation technologique .

Septembre 2012: IBM orchestre le lancement de la fondation OpenStack avec un investissement de 10 m\$ et 5600 membres transformant la dynamique des écosystèmes de Cloud ouverts



150+ interconnected OSS Projects

A l'ère d'une Smarter Planet, IBM continue à s'impliquer dans les écosystèmes Opensource....



A l'ère de l'e-business...

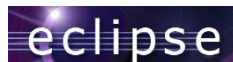
IBM tire parti de l'émergence du mouvement **open source** ...

30-50 OSS Projects

...et devient le leader du marché SOA et le premier éditeur de middleware



20-30 independent OSS Projects



Novembre 2001 – IBM fédère 150 éditeurs et une communauté de développeurs autour d'une nouvelle plateforme de développement logiciel, et contribue pour 40m\$ de code ,source. Cette initiative bouleverse le marché du développement logiciel



Septembre 1999: IBM investit 60m\$ annuellement sur Linux, et devient un membre actif de la communauté développant Linux



Apache

Juin 1998 – IBM signe un accord de technologie avec The Apache Group pour le développement du serveur HTTP Apache,



You know what's cool?

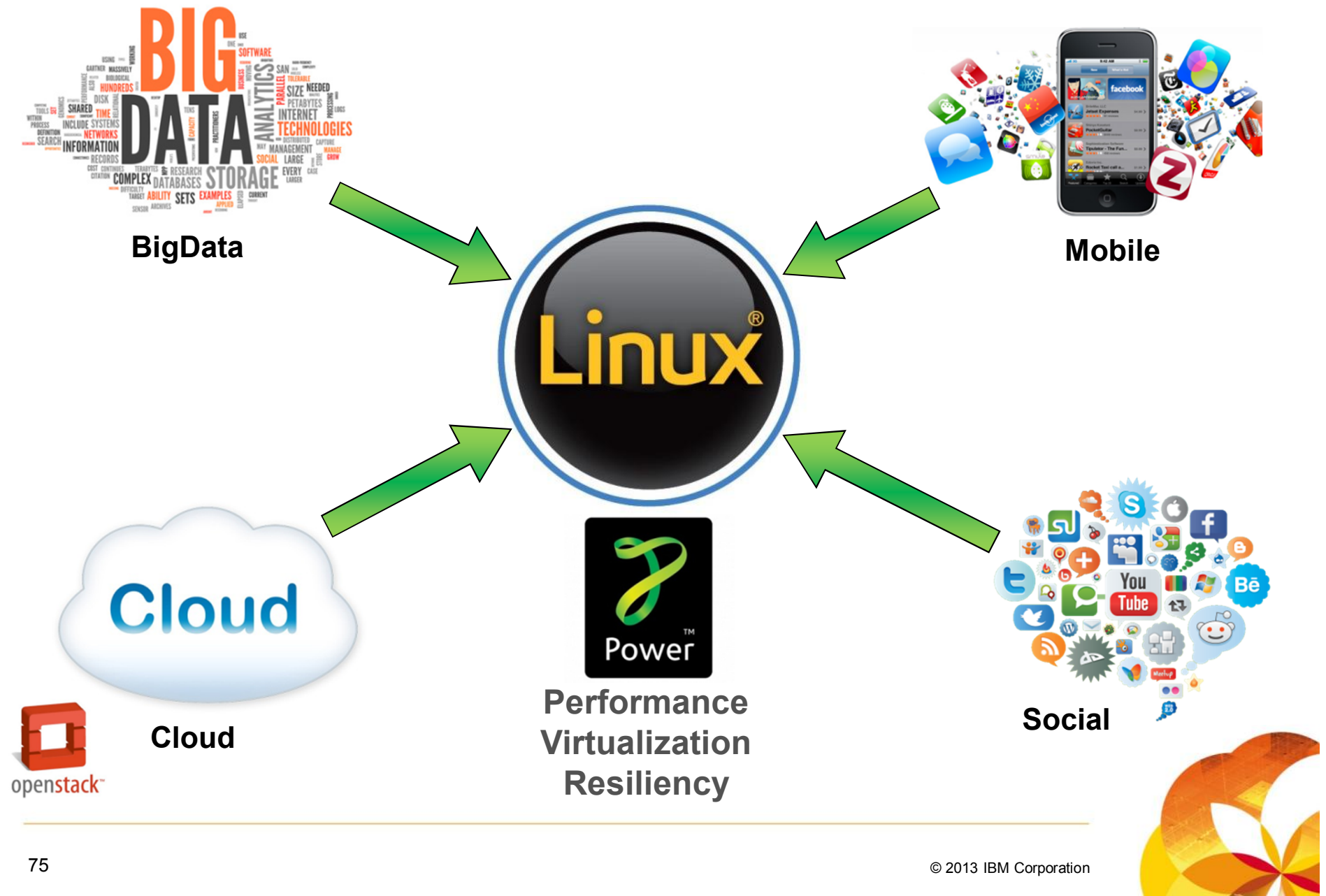
\$1 Billion

Power Systems intends to invest **a billion dollars** in solutions for Linux and open source workloads, adding to prior investments by IBM during the last decade on a wide range of open initiatives.

In addition, we're expanding our **Linux on Power development cloud**, which will give Linux developers who want to prototype applications easy access to Power.

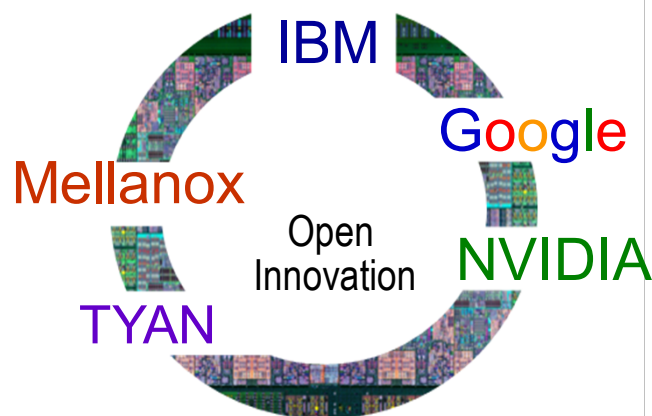
Finally, we're opening a new **Power Systems Linux Center** in Montpellier, France, joining a worldwide network of centers dedicated to the success of Linux software developers on Power.

Offering POWER to new OpenSource Workloads



Ecosystem leadership providing client choice and flexibility

OpenPOWER Consortium



- Collaborative innovation for highly advanced systems
- Produce open hardware, software, firmware and tools
- Expand industry skills and investment for Power ecosystem
- Provide alternative architectures

Open Applications and Tools



- JavaScript
- OpenJDK



- Access to industry innovation from a broad community
- Optimize scripting languages and development tools
- Contribute innovation to Linux, KVM and OpenStack

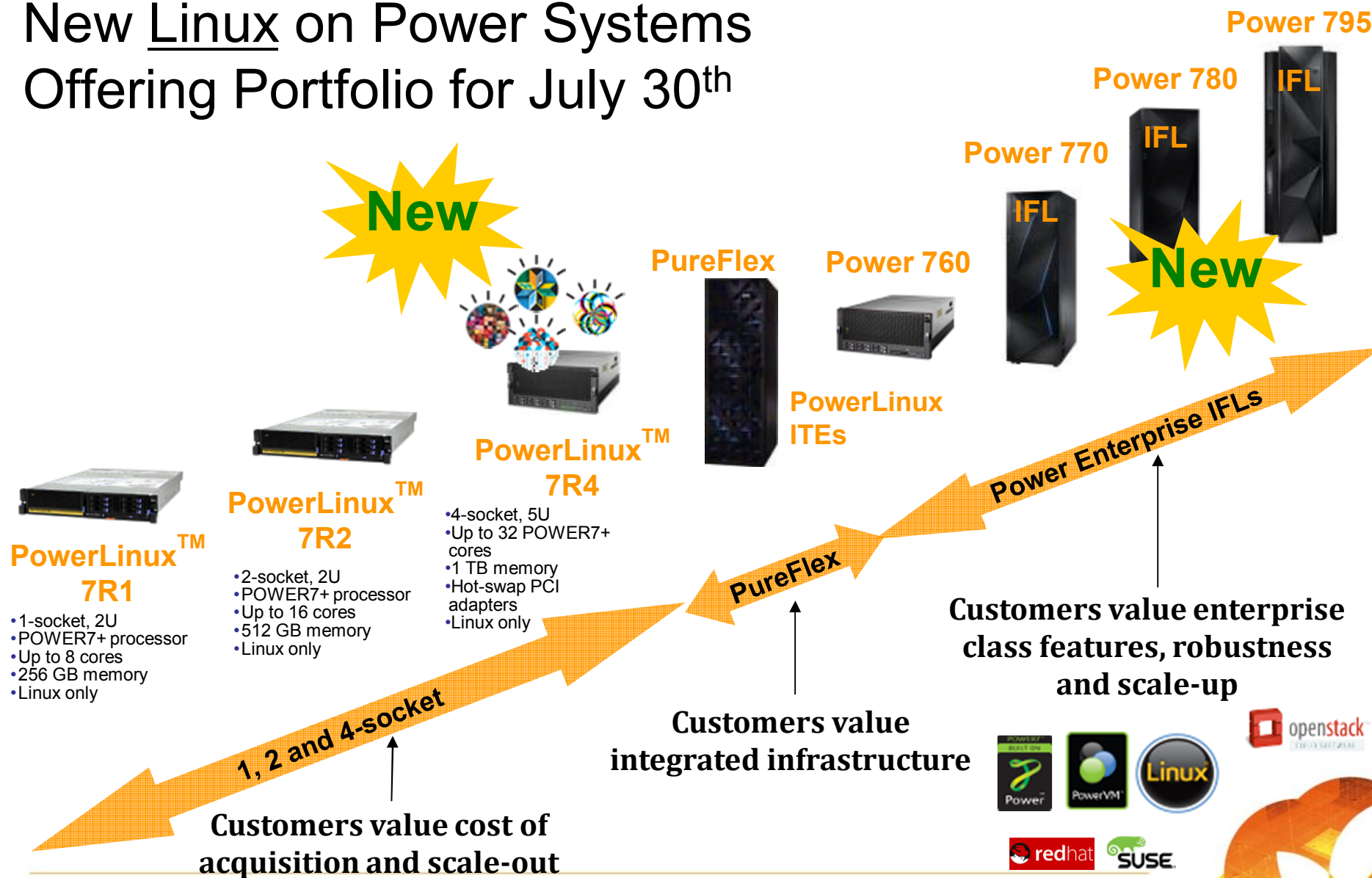
Open Management



- Simplified, consistent management
- Software-defined environments
- Deployment on premise or via cloud
- Seamless upgrades



New Linux on Power Systems Offering Portfolio for July 30th



Now Four Types of Activations

Static	Mobile Annc Oct 2013	Elastic or On/Off CoD	Power IFL Annc Oct 2013
Permanent activation	Permanent activation	Temporary activation ★	Permanent activation
AIX, IBM i, Linux	AIX, IBM i, Linux	AIX, IBM i, Linux	Linux only ★
PowerVM choice Standard or Enterprise across all server	PowerVM choice Standard or Enterprise across all server	PowerVM choice Standard or Enterprise across all server	PowerVM Enterprise only, PowerVM for PowerLinux for Power IFL ★
Supported on all Power 770/780/795	- 795 in 4Q 2013 - POWER7+ 770 / 780 Apr 2014 ★	Supported on all Power 770/780/795	Supported on all Power 770/780/795
Many firmware levels	Newest 780 firmware ★	Many firmware levels	Many firmware levels
Base cost ★	More value ★	Temporary ★	Lowest cost ★

Additional temporary
activations: Utility CoD and
Trial Cod not shown



PowerVM for IBM PowerLinux™ vs. VMware - \$ US

Superior capabilities and value – dynamically add or remove resources and **save 16%**



16%

<u>Virtualization features</u>	PowerVM for IBM PowerLinux⁴	VMware vSphere 5.0 – Enterprise¹
Server platforms supported	PowerLinux 7R1 or 7R2 IBM Flex System p24L	x86-64 based servers
Guest operating systems supported	Linux	Linux, Windows, Solaris and others
<u>Memory</u> - dynamically add or remove	Yes	Add – Yes Remove - No
<u>Virtual CPUs</u> - dynamically add or remove	Yes	Add – Yes Remove – No OS support
Virtual CPUs per VM	Only limited by # cores 7R1: 32 7R2/p24L: 64 795: 1,024	32 per socket (limited by Enterprise Ed. license)
Secure hypervisor (zero reported vulnerabilities)	Yes (h/w based)	No (s/w based)
License + 3 year, 9x5 SWMA 	\$7,840³ (2-sockets / 16 cores)	\$9,374² (2-socket / 64 vCPU license)

¹VMware edition comparisons: www.vmware.com/products/datacenter-virtualization/vsphere/compare-editions.html

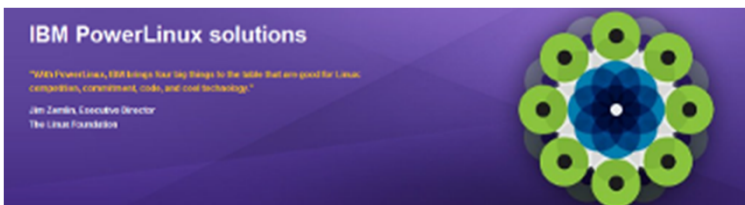
²VMware pricing: www.vmware.com/products/datacenter-virtualization/vsphere/pricing.html

³Based on US pricing for PowerVM for PowerLinux as of 10/05/2012

⁴PowerVM for PowerLinux is functionally equivalent to PowerVM Enterprise Edition & is only available for Linux only, PowerLinux servers.

Linux on Power Big Data Analytic Innovation

Faster +64%



- Big Data Analytics Innovation
 - IBM PowerLinux Big Data Solution for Apache Hadoop
 - New benchmark: only use 1/3 the time to sort 1TB of data vs. comparable x86 cluster
- IBM PowerLinux Advantages
 - POWER7 has 4 SMT per core vs. Intel's 2 threads per core
 - POWER7 has outstanding memory and I/O bandwidth
 - POWER7 offers highly optimized JVM
 - POWER7 servers deliver high I/O bandwidth



8 min 44s



10 Power7R2+1 EXP24S

24 min



one result used 10 x86 Linux nodes and another used 11 x86 Linux nodes*

*MapR used 1 master node and 10 slave nodes for its Terasort results (@Hadoop Summit 2011). Cloudera used 10 nodes (@Hadoop World 2011).



New IBM PowerLinux™ 7R2 pricing comparison (\$US)

Server list price* -3-year warranty, on-site	\$10,483	\$11,946	\$11,628
Virtualization - OTC + 3yr. 9x5 SWMA	\$9,374 VMware vSphere Enterprise 5.1	\$9,374 VMware vSphere Enterprise 5.1	\$7,840 PowerVM for IBM PowerLinux
Linux OS list price - RHEL, 2 sockets, unlimited guests, 9x5, 3 yr. sub./ supp.	\$5,697 Red Hat subscription and Red Hat support	\$5,697 Red Hat subscription and Red Hat support	\$4,489 Red Hat subscription and IBM support
Total list price: Server/Virtualization/Linux	\$25,554	\$26,568	\$23,957



* Based on US pricing for PowerLinux 7R2 announced on 2/05/2013 matching configuration table below. Source: dell.com, hp.com, vmware.com: 1/15/13

Compare prices online



Server model	Dell R720	HP ProLiant DL380p G8	IBM PowerLinux 7R2
Processor / cores	Two 2.9 GHz , E5-2690, Sandy Bridge, 8-core processors		Two 4.2 GHz POWER7+, 8-core
Configuration	32 GB memory, 2 x 147GB HDD, 10 Gb two port		Same memory, HDD, NIC



TCA pricing of Power vs. Intel x86 for Linux is comparable

PowerLinux 7R1 vs. Dell R720

(Comparable 1-socket server w/ virtualization & Red Hat)

Dell PowerEdge
R720

\$16,935



IBM PowerLinux
7R1

\$15,404



PowerLinux 7R2 vs. HP DL380 G8

(Comparable 2-socket server w/ virtualization & Red Hat)

HP ProLiant
DL380 G8

\$27,707



IBM PowerLinux
7R2

\$23,957



PowerLinux 7R4 vs. HP DL580 G7

(Comparable 4-socket server w/ virtualization & Red Hat)

HP ProLiant
DL580 G7

\$67,439



IBM PowerLinux
7R4

\$67,435



Power IFLs vs. Intel x86 scale out

\$16,935



8-cores

\$27,707



16-cores

\$67,439



32-cores

Power IFL

\$8,591*
(4-cores)



\$78,280
(32-cores)



Activate 4 cores per
Power IFL

* Does not include Linux OS



Thank You



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*Power Systems
Systems & Technology Group
IBM Client Center
Montpellier - France*

...any Question ?

